PC-8700

SHARP SERVICE MANUAL

CODE: 00ZPC8900GSME

PERSONAL COMPUTER

PC-8700
MODEL PC-8900

OPTION : CE-871B
CE-872B
CE-873B
CE-871PR
CE-871HD
CE-872HD
CE-871EB

CONTENTS

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

【THE FOLLOWING CAUTION IS APPLICABLE IN THE UNITED STATES ONLY. 】
"BATTERY DISPOSAL"
"CONTAINS NICKEL-CADMIUM RECHARGEABLE BATTERY MUST BE RECYCLED OR DISPOSED OF PROPERLY. REMOVE THE BATTERY FROM THE PRODUCT AND CONTACT FEDERAL OR STATE ENVIRONMENTAL AGENCIES FOR INFORMATION ON RECYCLING AND DISPOSAL OPTIONS."

【THE FOLLOWING CAUTION IS APPLICABLE IN THE UNITED STATES ONLY. 】
"BATTERY DISPOSAL"
"CONTAINS NICKEL-METAL HYDRIDE RECHARGEABLE BATTERY MUST BE RECYCLED OR DISPOSED OF PROPERLY. REMOVE THE BATTERY FROM THE PRODUCT AND CONTACT FEDERAL OR STATE ENVIRONMENTAL AGENCIES FOR INFORMATION ON RECYCLING AND DISPOSAL OPTIONS."

CHAPTER 1. OUTLINE OF THE PC-8700/8900

1. General

1-1. System Overview

In a compact notebook-sized package, the system packs an incredible volume of PC performance and versatility. In fact, the system is equipped with more features than are found on many desktop computers.
All the components of this machine are enclosed in a sturdy plastic case. The ports and connectors which the system uses to connect to peripheral items and other systems are located on the right, left and rear panels of the case.
Place the system on a desk or table where you can examine it easily. Look at the front, side and rear panels of the system before you actually open it up. This way it will be easier to spin the machine round and examine each side in detail.

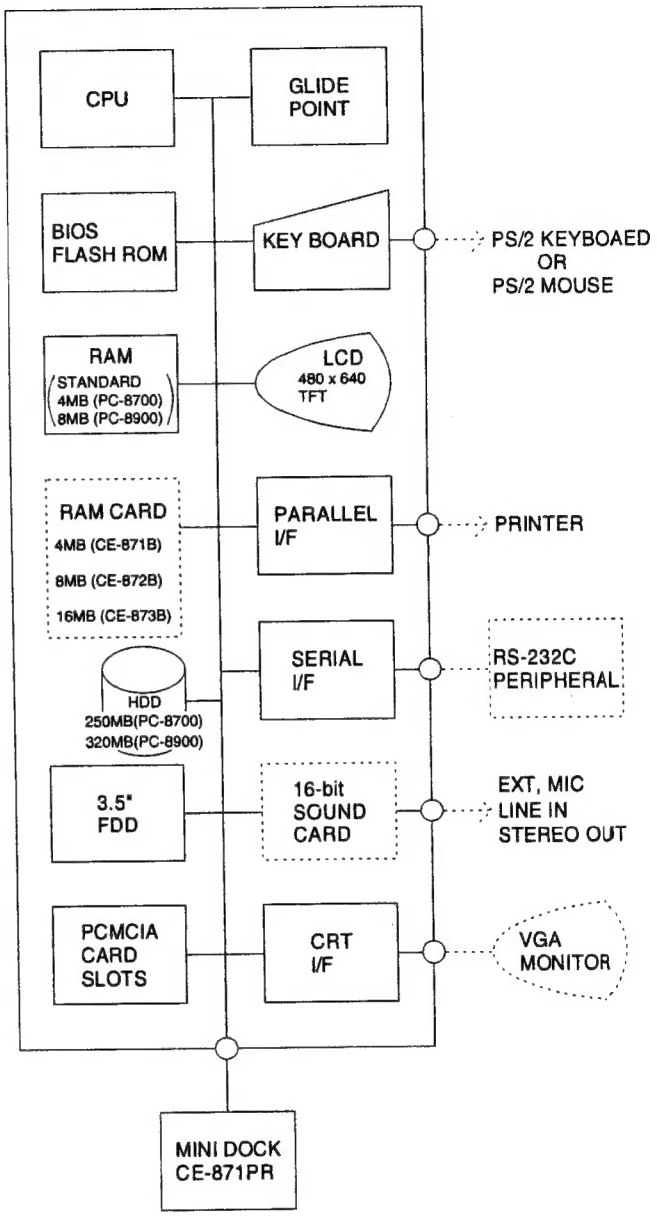
1-2. Feature Highlights

- Intel SL-Enhanced CPU i486 DX2/50 3.3V (PC-8700)
- Intel SL-Enhanced CPU intel DX4/75 3.3V (PC-8900)
- Standard 4MB Memory RAM. Expandable to 32MB (PC-8700)
- Standard 8MB Memory RAM. Expandable to 32MB (PC-8900)
- 32-bit VL-bus VGA controller with 1MB memory
- Built-in 16-bit Sound card, uni-directional microphone, speakers
- Advanced power management feature

Device

- Color 8.4" TFT LCD (640 x 480 dots) with backlight (PC-8700)
- Color 10.4" TFT-LCD (640 x 480 dots) with backlight (PC-8900)
- 3.5" 1.44MB/720KB Floppy Disk Drive
- 2.5" 250MB Hard Disk Drive (PC-8700)
- 2.5" 320MB Hard Disk Drive (PC-8900)
- PCMCIA Drive
- Optional Mini dock
- MS-DOS 6.22 and MS-Windows V3.11

1-4. System Configuration

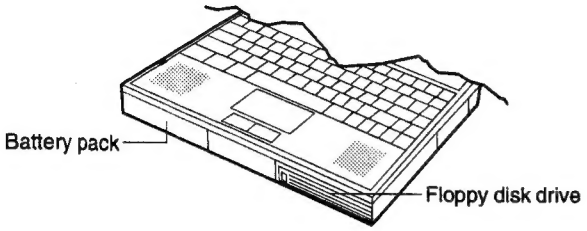


HDD (250MB)	CE871HD
HDD (320MB)	CE-872HD
Battery	CE-871EB

2. External View

(1) Front Panel

Look first at the front panel of your computer and you will see that it is installed with two modules. The left side module is the removable internal battery pack, known as the primary battery. The right side module is the removable floppy disk drive.



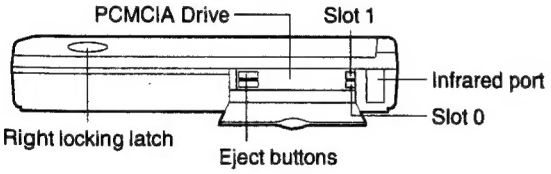
These are modular components that you can remove and replace easily. For example, you can carry a spare battery pack and use it to replace the primary battery when the primary battery is discharged. Or, if you don't often use the floppy disk drive, you can replace the floppy disk drive module with a second battery pack, known as an auxiliary battery.

Floppy Disk Drive

The floppy disk drive can read from and write to 3.5" diskettes with capacities of 1.44 MB or 720 KB. The disk drive has an eject button to eject diskettes from the drive.

(2) Right Panel

The right edge of your computer is the location of the PCMCIA drive and the infrared port.



PCMCIA Drive

You can open up the PCMCIA drive by pulling down the cover using the finger latch on the top edge of the cover. Inside the PCMCIA drive there are two type II PCMCIA slots. Type II slots are designed to be used by type I (3.3 mm thick) and type II (5 mm) PCMCIA cards.
The type II slots are stacked one on top of the other so you can also use a type III PC card (10.5 mm) in the lower slot, provided the upper slot is empty. On the left side of each slot there is an eject button.
The PCMCIA slot requires special software in order to operate correctly. Software, and utility programs to help you install and use a wide variety of cards, are provided on the system support diskette number two.

Right Locking Latch

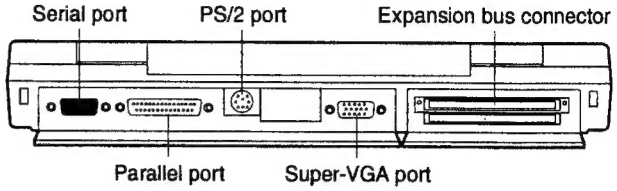
This latch, along with the corresponding latch on the left side, secures the upper cover screen assembly. To open the built-in LCD screen, slide the latches toward you and raise the system cover.

Infrared Port

The infrared port, identified as COM2, allows your computer to communicate with the Sharp Wizard Electronic Organizer as well as other devices with ASK infrared ports, without connecting any cables. You can transfer your organizer's data to your computer, modify the data using the PC's applications, and return the data back to the organizer.

(3) Rear Panel

The rear panel of the system has a connector compartment and an expansion compartment. Both compartments are protected by fold-down covers. You can pull the covers open by using the finger latches in the top edge of the compartment covers.



Connector Compartment

The connector compartment has four ports: a serial port, a parallel port, a PS/2 port, and a Super-VGA port.

Serial Port

The 9-pin serial (RS-232C) port is identified as COM1. You can use this port to connect your computer to devices which use serial communications, such as fax/modems, some pointing devices, and so on.

Note: If you want to use a serial mouse connected to the serial port, the GlidePoint should be disabled in the Setup utility.

Parallel Port

The 25-pin parallel port is identified as LPT1. The parallel port supports bi-directional parallel communications which is an industry standard parallel specification used by practically all parallel devices. You can also use the Setup utility to change the configuration of the parallel port to EPP (Enhanced Parallel Port) and ECP (Extended Capabilities Port). These are newer, faster parallel specifications which will be supported by the emerging generations of parallel devices.

PS/2 Port

The mini-DIN PS/2 port can be used by a PS/2 keyboard, or a PS/2 pointing device such as a mouse.

Caution: The GlidePoint in your computer also uses a PS/2 interface. If you want to install an external pointing device through the PS/2 port, you should use the Setup utility to disable the GlidePoint and avoid conflicts that may cause your computer to malfunction.

Super-VGA Port

The Super-VGA port can be used to attach an external VGA or Super-VGA monitor to your computer.

Expansion Compartment

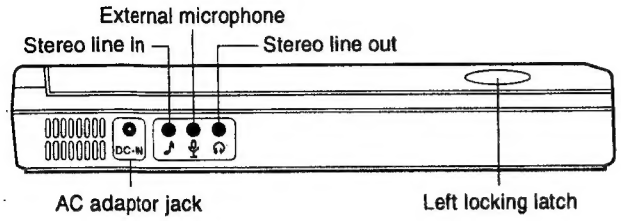
You can open the cover of the expansion compartment until it is horizontal and then slide the cover back into the computer so that it is out of the way while you use the expansion bus connector.

Expansion Bus Connector

The 200-pin expansion bus connector can be used to connect your computer to the optional CE-871PR Mini-Dock. Locking latches on the Mini-Dock fit into the two oval holes on the right and left of the rear panel of your computer.

(4) The Left Panel

On the left edge of your computer you will find the AC adaptor jack and the external audio jacks.



AC Adaptor Jack

This jack is the power input port for the AC adaptor. The AC adaptor converts local AC power into a DC supply which can be used to power the system and also to charge the internal battery pack.

Audio Jacks

Your computer is installed with a 16-bit stereo sound card, stereo speakers, and a built-in microphone. These jacks can be used to connect external audio equipment to your computer. When you connect an external device to the stereo line in or out, the built-in device (either microphone or speakers) will be disabled.

Microphone Jack

The microphone jack connects an external microphone.

Stereo Line In

The stereo line in records sound from an external source.

Stereo Line Out

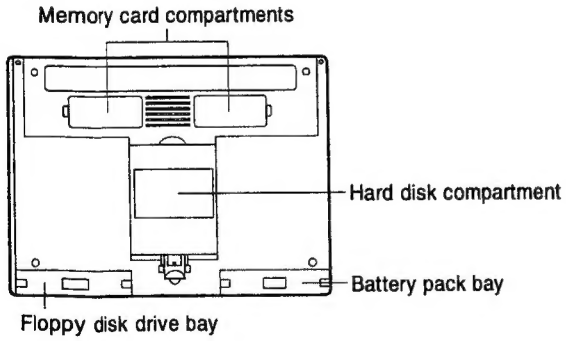
The stereo line out plays the computer's sound output on external loudspeakers or headphones.

Left Locking Latch

This latch, along with the corresponding latch on the right side secures the upper cover/screen assembly. To open the built-in LCD screen, slide the latches toward you and raise the system cover.

(5) The Computer's Base

Through the base of your computer's cabinet, you can access the floppy disk drive and battery pack bays, the hard disk drive compartment, and the two memory card compartments.



Floppy Disk Drive Bay

You can remove the floppy disk drive module from your computer and replace it with an optional extra battery pack (CE-871EB).

Battery Pack Bay

The replaceable battery pack is a self-contained module that installs into the bay on the front left-hand side of your computer. The battery pack uses Nickel-Metal Hydride cells.

Hard Disk Drive Compartment

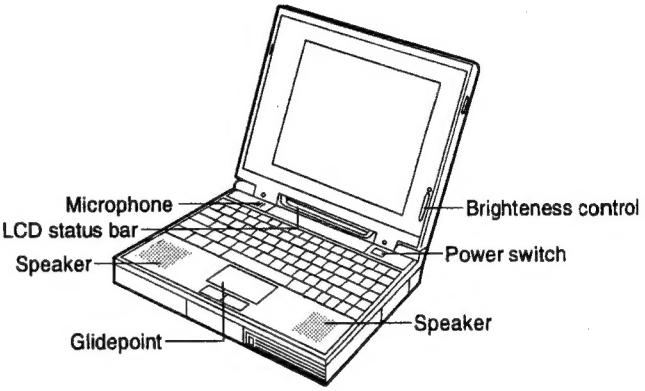
Your computer's operating system and other pre-installed software are stored on the removable hard disk drive.

Memory Card Compartments

There are two memory card compartments. In a standard configuration, the left side memory compartment is occupied by a 4 MB memory card (PC-8700) or an 8 MB memory card (PC-8900).

3. Internal View

You can use the latches on the right and left sides of the computer to unlock the upper cover screen assembly and open up your computer.



Microphone

A microphone has been installed in the round indentation just below the left screen hinge.

Speakers

Left and right stereo loudspeakers have been installed in front of the keyboard on either side of the GlidePoint.

Power Switch

The power switch, located just above the keyboard, turns the system's power On and Off. This button controls all the power to the system regardless of whether you are using a battery or an AC power supply. Press the power button to turn the power On. Press the button again to turn the power Off.

GlidePoint

The GlidePoint is a touch sensitive pointing device located just in front of the keyboard. The pad of the GlidePoint is like a representation of your computer's built-in screen and you can move the screen pointer by moving your fingertip lightly across the pad.

(1) LCD Screen

Your computer's built-in screen uses a vibrant, active matrix LCD. It is fixed at a very high contrast level producing graphics with clear and vivid colors.

This LCD screen has a fast response time that can track and display even quite fast movements of the screen cursor when you are using the GlidePoint.

The system has 32-bit VESA local bus VGA graphics with 1 MB of video memory. The built-in LCD is a 640 x 480 pixel screen. Up to 256 colors can be displayed at a resolution of 1024 x 768 when an external monitor is connected to the system. The video controller supports Simulscan, a simultaneous display on the built-in screen and an external monitor.

The LCD screen is backlit. To save battery power, the system has a feature that powers down the LCD when it has not been used for a predetermined amount of time.

Brightness Control

A sliding switch below and to the right of the LCD screen is the brightness control for the display. This switch helps you to obtain the best possible screen visibility. Sliding the switch upward increases intensity, and sliding it downward decreases intensity. The switch is quite sensitive and requires careful positioning to obtain the best effect.

(2) LCD Status Bar

The LCD status bar uses icons to indicate your system's current mode or status. The icons are visible when a mode or feature is active.

This icon is visible when the keyboard is in Caps Lock mode.

This icon is visible when the keyboard is in Num Lock mode.

This icon is visible when the keyboard is in Scroll Lock mode.

The upper and lower frames of this icon are always shown. The appropriate frame will be filled in when a PC card is inserted in either the upper or lower of the PCMCIA slots. When a type III card is inserted, the lower frame is filled.

This icon is visible when the computer is accessing the hard disk.

Caution:
Never turn off the computer while the hard disk icon is visible. The hard disk may still be saving information for a few seconds even after your software indicates that it is ready.

This icon is visible when the computer is accessing the floppy disk.

Caution:
Never remove the floppy disk drive module or a diskette while the floppy disk icon is visible.

This icon is visible when the computer is in the suspend to RAM mode.

This icon is visible when the computer is powered by the internal battery. The battery icon will start flashing when there are only a few minutes of battery power left.

Caution:
When the battery icon begins to flash, save your work and turn off your computer or suspend your computer to disk immediately.

This iron is visible when the computer is powered by the AC adaptor.

(3) Keyboard

The layout of your computer's keyboard is similar to a normal keyboard. In addition, there are twelve function keys, cursor control keys, and other special function keys such as **Ctrl, Alt, Esc, Prt Sc, Pause, Pg Up, Pg Dn, Home** and **End**.
The Numeric Keypad is embedded in the right-of-center alphanumeric keys. The keypad is activated and deactivated by pressing the **Num Lock** key. The Num Lock iron appears when in Num Lock mode.

Special Key Combinations

Special key combinations allow you to use various functions of the computer easily.

With the Ctrl and Alt Keys

Ctrl + Alt + Delete

The **Ctrl + Alt + Delete** key combination halts all operation of your computer and commands it to reset. This is known as a "warm boot". The computer will halt current operations and restart afresh. This key combination may be useful if you encounter hardware or software problems which "lock up" your computer.

Caution: The use of the **Ctrl + Alt + Delete** key combination will result in the loss of all data in memory.

Ctrl + Alt + S

This key combination is a signal to the computer that you wish to view the Setup utility.

Ctrl + Alt + ↑

When this key combination is pressed you will hear a high pitched beep, this switches the CPU into a fast mode. In this mode the CPU uses its built-in cache memory. this is the default setting for the CPU.

Ctrl + Alt + ↓

When this key combination is pressed you will hear a low pitched beep, this switches the CPU into a slow mode. In this mode the CPU does not use its built-in cache memory.

Note: **Ctrl + Alt + S, Ctrl + Alt + ↑**, and **Ctrl + Alt + ↓** are functional only when in DOS.

With the Fn Key

The **Fn** key, in combination with other special keys, controls some of the computer's features. Symbols are printed on the keyboard to show the functions.

Fn + F2

This key combination opens up Page 2 of the Setup utility in both DOS or Windows. This page allows you to set up power management features.

Fn + F5

This key combination toggles the display between LCD, CRT, and Simulscan.

Fn + F8

This key combination decreases the volume of the audio system.

Fn + F9

This key combination increases the volume of the audio system.

Fn + F10

This key combination disables the Battery Low beep. Note that this combination disables the beep temporarily but does not change the data in the Setup utility.

Fn + F12

This key combination puts your computer into suspend mode (either to disk or to RAM).

Fn + Ctrl (No symbol)

This key combination returns the right Ctrl keystroke to your computer.

4. Software Specification

Setup Utility

The Setup utility stores the basic configuration of your computer in CMOS memory where it is maintained by the internal clock battery. Each time you turn on the system, the stored information provides a reference point for the Power On Self Test and initialization routine. The Setup utility consists of two pages.

Accessing the Setup Utility

Setup Utility Page 1

Open up Page 1 by pressing **Ctrl + Alt + S**. You can only enter this page only when you are in DOS. Before you enter this page, be sure that all your application programs are closed. Press **Pg Dn** or **Pg Up** to turn to Page 2.

Setup Utility Page 2

Press **Fn + F2** to open up Page 2 of the Setup utility whether in the DOS or Windows environment. There is no need to close any application that is running to make changes in this page. The **Fn + F2** key combination will not allow you view and modify Page 1. You can also enter Page 2 by pressing **Pg Dn** or **Pg Up** while on Page 1.

Making Selections

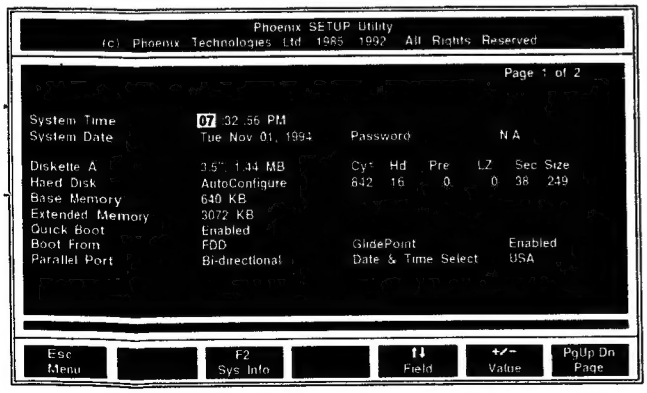
Use the arrow keys to move the cursor from one item to another. To select values for the selected item, use the **Spacebar**, **+** or **–** key. The **Spacebar** and **+** keys move forwards through the selection list while the **–** key moves backwards.

Exiting/Saving the Setup Utility

When in either one of the Setup screens, pressing the Esc key displays the Exit/Save menu.
Pressing Esc again returns to the Setup utility to make more selections.
Pressing **F5** reinitializes all settings to their default values. If you accidentally change the setup settings to incorrect values, your system may not operate correctly.
Pressing **F6** simply aborts the Setup utility without updating any of the settings you made.
The manner of saving and quitting the Setup utility depends on how you have entered it. If you entered the Setup utility using the **Ctrl + Alt** + S key combination, pressing **F4** saves, quits and reboots the system. This is necessary for the changes to take effect. If you entered the Setup utility Page 2 using the **Fn + F2** key combination, pressing **F4** saves and quits the Setup utility without having to reboot the system. The changes take effect immediately.

Setup Screen Page 1

The illustration below shows an example configuration of Page 1.



System Time / System Date

The system has a Realtime Clock/Calendar which is maintained by the clock battery. If the data and time need changing, highlight the items and set the correct time and date. You cannot change the seconds item except to reset the counter to zero. The day of the week is automatically updated as you change the other items.

Diskette A

This item refers to the floppy disk drive installed in your system. The system's factory-installed floppy disk drive is a standard 3.5" drive, and has a 1.44 MB capacity.

Hard Disk

Set this value to AutoConfigure so that your computer can automatically read the correct values of the cylinder, head, write precompensation, landing zone, sector, and size from the hard disk itself.

Base Memory / Extended Memory

These items refer to the RAM size you have available in your system. Under MS-DOS the Base memory is the memory up to 640 KB, so the value is always set to 640 KB. Extended memory is all memory above 1 MB expressed in KB (1 MB = 1024 KB). So if you have 4 MB RAM in your computer, Extended Memory will read 3072 KB. If you have 8 MB RAM, it will read 7168 KB.

Quick Boot

This item allows you to select a faster way of restarting your system. You should enable this item if you wish to skip the hardware diagnostic sequence of the POST.

Boot From

This item refers to the source of the DOS system command that is loaded into the system at start-up time. The system will look for the DOS system command either in the HDD or the FDD depending on the setting you have selected here. You will normally set this to HDD where your DOS system command is stored. However, for some purposes, you might want to boot a "clean" operating system from a floppy disk.

Parallel Port

As well as standard bi-directional parallel communication, the system supports an Enhanced Parallel Port (EPP) or an Extended Capability Port (ECP). Use this field to configure the port to whichever specification you need.

Password

The Password setting, if enabled, tells Setup to activate the security password feature. A user-specified password of not more than 7 characters will protect the system from unauthorized access. At every start up, a password prompt that asks you to enter your password will appear. The system will start the POST routine only after you have entered the proper password.

Setting up the Password

1. Highlight the Password item which shows N/A (Not Available) as the default value on Page 1 of the Setup utility. You will see the following message:

   `WARNING! Changes to this field will alter your POST Security Code. Press ENTER to Continue or any other key to exit without changes.`

2. Press Enter and the system will prompt the following message:

   `You may now enter the new password directly if you would like to set it.`

3. Type in a maximum of 7 alphanumeric characters as your password. A message prompting you to re-enter the password for verification will appear.

   `Reenter your password for verification.`

4. Re-write the password. If it is exactly the same as the first entry, the system will prompt the following message and will replace the "N/A" to "Enabled".

   ```
   New password is now installed. Press any key to
   continue.
   ```

   If the second entry is different from the first, the system will prompt the following message:

   ```
   Verification of your NEW password was
   incorrect! The original password remains
   unchanged. Press any key to continue.
   ```

5. Start over again. Be careful how you enter the password.

Change or Remove the Password

1. Open up the Setup utility Page 1 and highlight the Password item which shows "Enabled" and the system will prompt the following message:

   ```
   WARNING! Changes to this field will alter your
   POST Security Code. Press ENTER to Continue or
   any other key to exit without changes.
   ```

2. Press Enter if you wish to change the current password. The system prompts the following message after you press Enter.

   ```
   Enter the current Security Password for entry
   to this Field.
   ```

3. Enter your current password. Then, the system will prompt the following message:

   ```
   Verification of the old password was correct.
   You may now enter the new password or type F1
   to remove password security.
   ```

4. Enter the new password or press F1 to remove the password security. If you wish to change the password, follow steps 3, 4, 5 in the previous "Setting up the Password" section.

   Caution: If you forget the password, you will not be able to access the system. Always make a note of the password you have installed.

GlidePoint

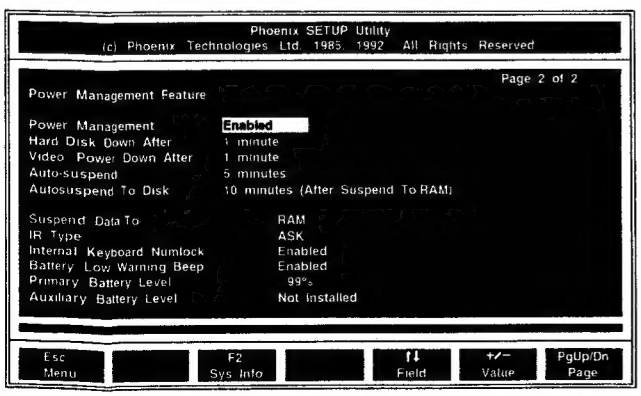
This item allows you to enable or disable the GlidePoint. You should disable the GlidePoint if you connect an alternative pointing device to either the PS/2 port or the serial port in the rear-panel connector compartment.

Date & Time Select

This item specifies the format of the System Time and Date. If you select USA, the time is shown using a 12 hour clock followed by AM or PM and the date appears as Day-Month-Date-Year. If you select Europe, the time is shown using a 24 hour clock and the date appears as Day-Date-Month-Year.

Setup Screen Page 2

The illustration below shows an example configuration of the Setup Screen page 2.



Power Management

On this page of setup, there are several user-controlled power down features. This item serves as the on/off switch for all the other power management features. If you set the value of this field to Disabled, all the power down features are turned off. If you set this field to Enabled, all the power down features are turned on. If you set this field to AC Disabled, the power down features are turned off while the computer is running on the AC adapter.

Hard Disk Down After

If the hard disk is not accessed for the user-specified time, the hard disk will power down. When the hard disk is next required, the drive will automatically be resupplied with power. Possible settings are Disabled and from 1 to 16 minutes.

Video Power Down After

If no keystroke or video activity takes place for the user-specified time, the LCD display will power down. Any keystroke will resume power to the LCD display. Possible settings are Disabled and from 1 to 16 minutes.

Auto-suspend

The Auto-suspend timer starts after the system enters the Video Power Down. The system will enter suspend mode automatically when the Auto-suspend time elapses. Your computer will suspend to RAM or suspend to disk according to the settings of the field Suspend Data To (see below). Possible settings are Disabled and from 5 to 60 minutes.

Auto-Suspend To Disk

If the field Auto-suspend is set such that it suspends your computer to RAM, you can use this field to automatically suspend to disk if the computer is inactive for the time specified in this field. The time in this field only begins counting after Auto-suspend (to RAM) has taken place. Possible settings are Disabled and from 10 to 120 minutes.

Suspend Data To

This item allows you to choose whether to suspend your current data to RAM or to disk when the system enters Suspend mode.

IR Type

This item allows you to choose the communication method of the infrared port. You can set this item to ASK, Disabled.

Internal Keyboard Numlock

If you are using an external keyboard, you might want to use the external keyboard's Num Lock key. This key toggles the keypad from numbers and numeric operators to cursor control and editing keys. Using the external keyboard Num Lock key might cause the built-in keyboard function to operate incorrectly. Use this field to disable the built-in keyboard's Num Lock key before using the Num Lock key on an external keyboard.

Battery Low Warning Beep

The audio system is programmed to beep intermittently when the system estimates that there are only a few minutes of the internal battery power left. You can enable or disable this function using this item.

Note: The Fn + F10 key combination will also disable the battery low beep. Using this keystroke will not affect the Setup data.

Primary Battery Level

This item shows how much charge is held in the internal battery. A fully charged battery is rated 100%, and an empty battery is rated 0%.

Auxiliary Battery Level

This item shows how much charge is held in the second battery (if installed). A fully charged battery is rated 100%, and an empty battery is rated 0%.

5. System Power Management

Most of the power management in your computer is transparent and automatic because it is controlled by the Windows and DOS power managers. For example, when your computer is idle for more than 16 seconds, the processor automatically drops its clock speed to zero. As soon as the computer is active again, the processor instantaneously returns to full speed.
In addition to this automatic operation, there are component power-downs and system suspend modes.

(1) Powerdowns

The powerdowns are all controlled by the Setup utility as described in the following chapter. They include a hard disk power down, a video power down, an auto suspend, and an auto suspend to disk. You can set these powerdowns as you wish so that when your computer is turned on but inactive, it will progressively reduce power consumption and finally turn off automatically.

Turning the Powerdowns On and Off

In Page 2 of the Setup utility, the Power Management feature can be set to Enabled, AC Enabled or Disabled. If you set it to Enabled, all the powerdowns will operate whether you are using the AC adaptor or the internal battery. If you set it to AC Disabled, powerdowns will only be activated when you are using battery power to run your computer. If you set this feature to Disabled, none of the powerdowns will operate whether using the AC adaptor or the internal battery.

Hard Disk Power Down

The hard disk powers down after a user-specified time elapses with no hard disk access. When the hard disk is next accessed, it will power on automatically.

Video Power Down

the LCD powers if there is no keystroke or video activity for a user-specified time. Any activity, a keystroke for example, will resume power to the LCD. If you are displaying to both an external monitor and the LCD, the LCD display and the VGA signal to the external monitor will power down.

Auto-suspend

The Auto-suspend field automatically puts the computer into suspend mode after a user-specified time has elapsed. The computer will suspend to RAM or disk according to the value of the field Suspend Data To in the Setup utility. If Video Power Down has been enabled, the Auto-suspend time does not begin counting until Video Power Down has been completed.

AutoSuspend To Disk

If the Suspend Data To field is set to Suspend to RAM, then the field above, Auto-suspend, will generate a suspend to RAM. You can use the AutoSuspend To Disk field to generate a suspend to disk, even when your computer is programmed to suspend to RAM. If Video Power Down and/or Auto-suspend are enabled, the AutoSuspend to Disk time does not begin counting until the system has completed the Video Power Down and/or Auto-suspend.

(2) Suspend Mode

There are two different suspend modes; suspend to RAM and suspend to disk. As a default your system is set to suspend to RAM. You can program the computer to suspend to disk or RAM by using the Suspend Data To item in the Setup utility.

Suspend to RAM

When the system suspends to RAM, a beep sounds as a signal, then the state of the computer is stored to RAM. All but a few essential components of your system power down. Pressing any key allows the computer to return to exactly the same state as it was when the suspend mode was activated. You can use suspend to RAM when you have to pause your computing but plan to resume working after a short interval.

Suspend to Disk

You can also configure your system to suspend to disk. The system preserves all the current application programs as a file in a "suspend-to-disk partition" on the hard disk drive. The system then turns off automatically. When you next turn on the system, it reads the file from the suspend-to-disk partition back into memory, so that your computer is returned to exactly the same state as it was when you suspended it.
Suspend to disk is a very useful feature. People who work in the Windows environment frequently open many applications and have them iconized on the Windows screen. It takes some time to get all these applications open and running, and normally they all have to be closed before the system can be turned off. If you use suspend to disk, you don't need to close the applications as the state of your system is saved to disk. When you next turn on your system, your Windows screen, with all the applications open, will be recreated in just a few seconds.

Suspend-to-Disk Partition

10 MB of your hard disk space has been reserved as the suspend-to-disk partition. This means you can safely suspend to disk if your computer has 4 or 8 MB of installed memory. If you install more than 8 MB of memory, you will have to create a new, larger suspend-to-disk partition as described.

Note: Do not touch the computer while the suspend to disk operation is proceeding.

Using the Suspend Modes

The system enters the Suspend modes under the following conditions:

- The **Fn + F12** key combination is pressed
- The timeout set in Auto-suspend and/or the timeout set in Auto-Suspend To Disk) elapses
- The LCD panel is closed while the video output of the system is displaying only on the LCD

The system resumes from the Suspend to RAM mode under the following conditions:

- Any key is pressed
- A modem card installed in the PCMCIA slot receives an incoming call

The system will beep as a signal that the system has resumed normal power. You will return to the application that was active before you entered the suspend to RAM mode.

Closing the LCD

If the video output of the computer is being displayed on the built-in LCD only, closing the cover without the power being switched off suspends the system. If you have set your system to suspend to RAM, you can resume power to the system by opening the cover and pressing any key. If you have set your system to suspend to disk, closing the cover will suspend all your data to the suspend-to-disk partition and turn off the system. When you next turn on your computer, it will be returned to the same application that was open before you closed the cover.

If the video output of your computer is being displayed on both an external monitor and the built-in screen closing the cover turns off the built-in screen.

If the video output of your computer is being displayed only on an external monitor, closing the cover has no effect.

Note: After closing or opening the cover, wait at least two seconds after the beep sounds before you next move the cover.

Caution: If you are using an external monitor and an external keyboard we strongly recommend that you do not close the cover of the computer. The thermal design of the computer assumes that the cover is open during operation. If the cover is closed during operation, your computer can generate excessive heat which can damage sensitive components.

Low Power During a Suspend to RAM

If your computer detects that battery power is critically low while it is suspended to RAM, it will automatically resume to full power, carry out a suspend to disk, and then turn off.

The Audio System in Suspend Modes

For technical reasons, the state of the audio system cannot survive a suspend to disk or A suspend to RAM. If your sound system is active when you suspend to RAM or disk, it will not resume activity when you resume the computer or turn it back on. You must restart the audio system manually.

Battery Changing in Suspend Mode

If you only have a primary battery (one battery) installed in your computer, you cannot change the battery while the computer is suspended to RAM. If you have a primary and an auxiliary battery installed in your computer, it is possible to suspend the computer to RAM and change one of the batteries without losing data.

(3) Windows Advanced Power Management

Windows provides you with Advanced Power Management which gives you effective power management while using the Windows environment.

From the Windows Program Manager, open up the Control Panel window. In this window you will see an icon of a battery and an AC plug labeled Power. Select this icon to display the Power window. From this window you can select advanced or standard power management, or disable the power management. The window also displays a battery meter.

The Power window also has a help button. Select this to display help screens which fully explain Windows power management.

6. Power On Testing

The following terms are used in the Power On Testing table:

Pattern Test

One or more particular patterns are written to a location then read back from the same location. Examples of patterns used are 55h and AAh. If the value read does not match the value written, the test is considered a failure.

Rolling Ones Test

Several patterns are constructed. These patterns re[resent a one rolling through the given location. For example, to roll a one through three bits, the following patterns would be constructed: 001, 010, 011, 100, 101, 110, and 111. The patterns are written to the location and then read back, one by one. If the value read does not match the value written, the test is considered a failure.

Checksum Test

All of the values in a given range of locations are added together. The range includes a location which, when added to the sum of the ranges, will produce a known result, such as zero (0).

Beep Codes for System Errors

Beep Code	Diagnostic Code	Description	Test Performed
None	01h	CPU register test in progress or failure	Pattern test of most of the 16-bit CPU registers. Failure will result in a system halt.
1-1-3	02h	CMOS write/read test in progress or failure.	Rolling ones test in the shutdown byte (offset 0Eh) of the CMOS RAM. Failure will result in a system halt.
1-1-4	03h	ROM BIOS checksum test is in progress or failure.	The range of ROM that includes the BIOS is checksummed. Failure will result in a system halt.
1-2-1	04h	Programmable interval timer 0 test in progress or failure	Over a period of time, the current count values in timer 0 are read and accumulated by ORing them into the values read so far. It is expected that during the time period, all bits will be set. Failure will result in a system halt.
1-2-2	05h	DMA channel 0 address and count register test in progress or failure.	Rolling ones and rolling zeros test of the address and count registers of DMA channel 0. Failure will result in a system halt.
1-2-3	06h	DMA page register write/read test in progress or failure.	Pattern test of DMA page registers. Failure will result in a system halt.
1-3-1	08h	RAM refresh verification test in progress or failure.	Over a period of time, the refresh bit (bit 4) in port 60h is read and tested. The refresh bit should toggle from 0 to 1, then 1 to 0 within the time period. Failure will result in a system halt.
None	09h	First 64K RAM test in progress.	No specific test is performed — just indicates that the test is beginning (i.e., no failure).
1-3-3	0Ah	First 64K RAM chip or data line failure, multi-bit.	The first 64K of RAM is tested with a rolling ones test and pattern test. If any of the pattern tests fail, then the BIOS reports that multiple data bits failed (see specific bit tests following). Failure results in a system halt.
1-3-3	0Dh	Parity failure first 64K RAM.	At the completion of the rolling ones and pattern tests of the first 64K, the BIOS checks the parity error bits (bits 7 and 6) of port 60h. Failure results in a system halt.

Beep Code	Diagnostic Code	Description	Test Performed
2-1-1 2-1-2 2-1-3 2-1-4 2-2-1 2-2-2 2-2-3 2-2-4 2-3-1 2-3-2 2-3-3 2-3-4 2-4-1 2-4-2 2-4-3 2-4-4	10h-1Fh	First 64K RAM chip or data line failure on bit x (see test description).	The first 64K of RAM is tested with a rolling ones test and a pattern test. If any of the rolling ones tests fail, then the BIOS reports the specific bit that failed. To determine the bit number from the diagnostic code, subtract 10h. For example, if 15h is displayed at the diagnostic port, bit 5 failed. Failure results in a system halt.
3-3-1	20h	Slave DMA register test in progress or failure.	Pattern test of channels 1 through 3 of the slave controller (starting port address = 2). Failure results in a system halt.
3-1-2	21h	Master DMA register test in progress or failure.	Pattern test of channels 1 through 3 of the master DMA controller (starting port address = C4h). Failure results in a system halt.
3-1-3	22h	Master interrupt mask register test in progress or failure.	Rolling ones and zeros tests of the mask register of the master programmable interrupt controller (port 21h). Failure results in a system halt.
3-1-4	23h	Slave interrupt mask register test in progress or fail;ure.	Rolling ones and zeros tests of the mask register of the slave programmable interrupt controller (port A1h). Failure results in a system halt.
None	25h	Interrupt vector loading in progress.	No specific test is performed — just indicates that the Interrupt Vector table is being initialized (i.e., no failure).
3-2-4	27h	Keyboard controller test in progress or failure.	The self-test command (AAh) is issued to the 8042 (keyboard controller) and the results are monitored. Failure results in a system halt.
None	28h	CMOS RAM power failure and checksum calculation test in progress.	The power-fail bit in CMOS RAM is tested and the lower CMOS RAM area is being checksummed. A failure does not result in a system halt.
None	29h	CMOS RAM configuration validation for video in progress.	No specific test is performed — just indicates that the configuration specified in CMOS for video is being matched against the actual installation. A failure does not result in a system halt.
3-3-4	2Bh	Screen memory test in progress or failure.	The video buffers (B0000h and B8000h) are tested with a pattern test and a rolling ones test. Failure will result in a beep code but not a system halt.
3-4-1	2Ch	Screen initialization in progress.	Until the video installation is confirmed, any calls to INT 10h Function 0 (set mode) will be prefaced with this diagnostic code. There is no expected failure from this.
None	2Eh	Search for video ROM in progress.	No specific test is performed by the system BIOS — just indicates that the BIOS is about to jump to the initialization code in the video option ROM.
None	30h	Screen running with video ROM.	No specific test is performed — just indicates that a video option ROM was found and is believed to be operating.

Beep Code	Diagnostic Code	Description	Test Performed
None	31h	Monochrome monitor operable	No specific test is performed — just indicates that the BIOS believes a monochrome monitor is installed and is operating.
None	32h	Color monitor (40 column) operable	No specific test is performed — just indicates that the BIOS believes a color monitor is installed and is operating. The mode has been set to 40-column as selected by the user in CMOS RAM.
None	33h	Color Monitor (80-column) operable	No specific test is performed — just indicates that the BIOS believes a color monitor is installed and is operating. The mode has been set to 80-column as selected by the user in CMOS RAM.
4-2-1	34h	Timer-tick interrupt test in progress or failure.	All interrupts except the timer-tick interrupt are masked off at the interrupt controllers. If a timer-tick interrupt does not occur during a specific timer period, an error message is displayed on the screen. The system does not halt.
4-2-2	35h	Shutdown test in progress or failure.	A return address is stored in 40:67h and the processor is reset via the keyboard controller. If a timer-tick occurs during this time period, an error message is displayed on the screen. Other failures are hard to detect. If possible, the BIOS will continue with POST, skipping the memory tests.
4-2-3	36h	Gate A20 failure.	To test exteded memory, the processor must be placed in protected mode and the A20 line must be enabled. For the memory tests, the BIOS generally uses the keyboard controller to enable A20. If the A20 line is not properly set during the memory tests, an error message is displayed on the screen and the memory tests are suspended. The system does not halt.
4-2-4	37h	Unexpected interrupt in protected mode.	During the memory tests, the processor is placed in protected mode. All interrupts in the interrupt descriptor table are initialized to point to a special handler that displays a message on the screen. All hardware interrupts are masked off and interrupts are disabled. The system does not halt when such an unexpected interrupt occurs.
4-3-1	38h	RAM test of memory above 64K in progress or failure.	The memory above the first 64K is tested with a rolling ones test and a pattern test. All success and failure messages are displayed on the screen and POST will continue.
4-3-2	3Ah	Programmable interval timer channel 2 test in progress or failure.	Over a period of time, the current count values in timer 2 are read and accumulated bu ORing them into the values read so far. It is expected that during the time period, all bits will be set. If an error is detected, an error message will be displayed on the screen and POST will continue.
4-3-4	3Bh	Real-time clock test in progress or failure.	Over a period of time, the Update-In-Progress bit of Status register A of the real-time clock is read and tested. The bit should toggle from 0 to 1 within the time period.

Beep Code	Diagnostic Code	Description	Test Performed
4-4-1	3Ch	Serial port test in progress or failure.	Pattern test of one or more of the installed serial ports. If a failure is detected, an error message will be displayed and POST will continue.
4-4-2	3Dh	Parallel port test in progress or failure.	Rolling ones test is done to one or more of the installed parallel ports. If a failure is detected, an error message will be displayed and POST will continue.
4-4-3	3Eh	Math coprocessor test in progress or failure.	An integer load and store is performed with the math coprocessor. If the values do not match, an error message will be displayed and POST will continue.

7. Bios Messages

The Power On Self Test (POST) is the system test and component initialization process performed by the ROM BIOS in the computer. The central hardware is tested and initialized first.
Proper functioning of the central hardware is required before further system tests can be run. In general, a failure in a test of the system board or its components will sound a beep, and halt the system. A failure in add-on boards or memory is reported on the screen.
There are two types of messages POST displays:

- Error messages indicating a failure in either the hardware, software or firm ware.
- Informational messages about the power-on and booting processes.

POST messages are listed below, with possible causes and solutions.
Messages which do not appear in this list indicate hardware faults which can only be rectified by internal checks.

POST Error Messages

`Diskette drive (x) failure`

Possible cause The floppy disk drive has failed.

Solution Run the diagnostics program to check the floppy disk drive.

`Diskette read failure`

Possible cause The diskette is either not formatted or defective.

Solution Replace with a formatted diskette.

`Fixed disk configuration error`

Possible cause The setting of Hard Disk in the Setup utility is wrong.

Solution Run the Setup utility and enter the correct values.

`Fixed disk failure`
`Fixed disk controller failure`

Solution Reboot. If this does not work, run the diagnostics program to check the hard disk drive.

`Fixed disk read failure`

Possible cause The hard disk is defective.

Solution Reboot. If this does not work, run the diagnostics program to check the hard disk.

`Gate A20 failure`

Possible cause The system board is defective.

`Invalid configuration information - please run SETUP program`

Possible causes
Memory size is incorrectly configured.
Incorrect number of hard disk.

Solution Check the settings in the Setup utility.

`I/O card parity interrupt at xx`

Possible cause The system board is defective.

Solution Reboot.

`Keyboard clock/data line failure`

Possible cause The keyboard data line is defective.

`Keyboard failure`
`Keyboard controller failure`

Solution Reboot. If this does not work, run the diagnostics program to check the keyboard.

`Keyboard stuck key failure`

Possible cause One or more keys were pressed during the power-on self test.

Solution Avoid pressing any keys during the power-on self test except the **Space Bar** to terminate the memory test.

`No boot device available`

Possible cause Either the hard disk drive, the floppy disk drive, the diskette itself, the PCMCIA slot, or the IC card itself is defective.

Solution Reboot. If this does not work, replace with a bootable diskette or IC card. If you suspect the hard disk is faulty, run the diagnostics program.

`No boot sector on fixed disk`

Possible cause The hard disk is not formatted.

Solution Format the hard disk. Remember this wil erase the contents of the hard disk.

`Non-System disk or disk error`
`Replace and press any key when ready`

Possible cause The diskette in the floppy disk drive or the IC card in the PCMCIA slot is not formatted as a bootable diskette or IC card.

Solution Remove the diskette or the IC card, or replace with a bootable diskette or IC card and press any key.

`Not a boot diskette`

Possible cause The diskette in the floppy disk drive or the IC card in the PCMCIA slot is not formatted as a bootable diskette or IC card.

Solution Remove the diskette or the IC card and reboot.

`Time-of-day not set - run SETUP utility`

Possible cause The RTC time-of-day clock chip has failed.

Solution Reset the time and date in the Setup utility.

POST Informational Messages

`XXX Conventional Memory, XXXXXK Extended`

Meaning This message indicates the amount of memory that has tested successfully.

`Memory tests terminated by keystroke`

Meaning This message indicates that you have pressed the **Space Bar** while the memory tests were running. This stops the memory tests.

`Press F1 to retry boot, F2 for SETUP utility`

Meaning This message indicates that an error was found during the power-on tests. Pressing **F1** allows the system to attempt to boot, and pressing **F2** brings you to the setup utility.

`Press the F1 key to continue, F2 to run the SETUP utility`

Meaning This message indicates that an error was found during the power-on tests. Pressing **F1** allows you to start the system, ignoring the error, and pressing **F2** brings you to the setup utility.
You should press **F2** and enter the Setup utility.

CHAPTER 2. SPECIFICATIONS

Standard System

Main Unit

Size:	11.6″ (W) x 8.9″ (D) x 2.0″ (H) 295 mm (W) x 225 mm (D) x 50 mm (H)
Weight:	Approx. 6.2 lbs (2.8 kg) (including battery)
Power Source:	Ni-MH Battery/AC adaptor
Temperature Operating:	10°C to 35°C (50°F to 95°F)
Storage/Transit:	–20°C to 60°C (–4°F to 140°F)
Humidity Operating:	20% to 80%
Storage/Transit:	10% to 90%

Battery Pack

Ni-MH removable battery module

Size:	4.2″ (W) x 4.8″ (D) x 0.9″ (H) 106 mm (W) x 123 mm (D) x 24 mm (H)
Weight:	1.2 lbs (535 g) (including cover)
Capacity:	25.92 wh

AC Adaptor

Input:	100V ~ 250V AC, 47 ~ 63 Hz auto sensing
Output:	28.35 W DC Power Supply
Size:	2.3″ (W) x 4.6″ (D) x 1.4″ (H) 59 mm (W) x 118 mm (D) x 35 mm (H)
Weight:	0.6 lbs (270 g) (without AC cord)

AC cord is detachable from AC adaptor

Processor

PC-8700 SL Enhanced i486DX2 at 50 MHz
PC-8900 SL Enhanced i486DX4 at 75 MHz

RAM

PC-8700 4 MB RAM standard
PC-8900 8 MB RAM standard

ROM

ROM for IPL, BIOS, POST, Setup utility, and VGA-BIOS

Hard Disk Drive

PC-8700 Removable 2.5″ 250 MB hard disk
PC-8900 Removable 2.5″ 320 MB hard disk

Floppy Disk Drive

Removable 3.5″ 1.44 MB 2HD (720 KB 2DD) floppy disk drive

PCMCIA Drive

2 Type II specification slots or 1 Type III specification slot for PC memory and I/O cards

Glide Point

PS/2 mouse compatible
Touch sensitive pointing device with 2 buttons

Audio Output

output for stereo line out

Audio Input

2 inputs for external microphone, stereo line in

Speaker

Diameter: 40 mm

Microphone

Internal microphone for audio system

Infrared Port

Infrared communication port using ASK

Super VGA Port

15-pin D-SUB analog connector

Parallel Port

Centronics interface 25-pin female D-SUB

Serial Port

RS-232C interface 9-pin male D-SUB connector full duplex asynchronous transmission at up to 9600 baud

Expansion Bus Connector

200-pin connector for the optional CE-871PR Mini-Dock

Screen

PC-8700

8.4″ Illuminated active matrix color liquid crystal display

Text Display:	25 lines x 80 characters
Graphics:	640 x 480 pixels bitmapped
Color:	256 colors
Viewing Area:	6.7″ x 5.1″ (171 mm x 130 mm)

PC-8900

10.4 Illuminated active matrix color liquid crystal display

Text Display:	25 lines x 80 characters
Graphics:	640 x 480 pixels bitmapped
Color:	256 colors
Viewing Area:	8.3″ x 6.2″ (211 mm x 158 mm)

Keyboard

85 (U.S. Keyboard only)/86 keys including:
12 programmable function key capacity
Fn key
All 101/102 keys on the IBM enhanced keyboard are supported

Options

Memory Cards

CE-871B

4 MB Memory Card

Size:	2.4″ (W) x 1.1″ (D) x 0.2″ (H) 61 mm (W) x 29 mm (D) x 5 mm (H)
Weight:	0.02 lbs (8 g)

CE-872B

8 MB Memory Card

Size:	2.4″ (W) x 1.1″ (D) 0.2″ (H) 61 mm (W) x 29 mm (D) x 5 mm (H)
Weight:	0.02 lbs (8 g)

CE-873B

16 MB Memory Card

Size:	2.4″ (W) x 1.1″ (D) x 0.2″ (H) 61 mm (W) x 29 mm (D) x 5 mm (H)
Weight:	0.02 lbs (8 g)

Extra Battery Pack

CE-871EB

Ni-MH battery pack

Size:	4.2″ (W) x 4.8″ (D) x 0.9″ (H) 106 mm (W) x 123 mm (D) x 24 mm (H)
Weight:	1.2 lbs (535 g) (including cover)
Capacity:	25.92 wh

Mini-Dock

CE-871PR

Built-in SCSI port, MID/Game port, 2 PCMCIA Slots (type I, type II, type III compatible), 2 serial ports, parallel port, SVGA port

Size:	11.6″ (W) x 6.1″ (D) x 1.6″ (H) 295 mm (W) x 154 mm (D) x 41 mm (H)
Weight:	2.3 lbs (1.1 kg)

Hard Disk Drive

CE-871HD

250MB hard disk drive

Size:	2.9″ (W) x 5.4″ (D) x 0.6″ (H) 73 mm (W) x 137 mm (D) x 15 mm (H)
Weight:	0.35 lbs (160 g)

CE-872HD

320MB hard disk drive

Size:	2.9″ (W) x 5.4″ (D) x 0.8″ (H) 73 mm (W) x 137 mm (D) x 21 mm (H)
Weight:	0.49 lbs (220 g)

CE-873HD

500MB hard disk drive

Size:	2.9″ (W) x 5.4″ (D) x 0.8″ (H) 73 mm (W) x 137 mm (D) x 21 mm (H)
Weight:	0.49 lbs (220 g)

CHAPTER 3. DISASSEMBLY AND ASSEMBLY INSTRUCTIONS

A. Precautions

Before disassembly, remove the AC adaptor and the internal battery. Some components are very small so use a tidy worktable and store removed screws carefully.

B. Remove the Palmrest/Glidepoint Assembly, the Keyboard and the Audio Card Assembly

1. Close the upper cover and turn the unit over.
2. Remove the floppy diskette drive module and the internal battery.
3. Remove the two screws located inside the battery bay, and the two screws inside the diskette drive bay.
4. Turn the unit back over and open up the upper cover.
5. Reach inside the battery bay and insert a finger into the hole in the top of the battery bay. This hole allows you to push upward on the palmrest/glidepoint assembly and snap it free from the unit base.
6. Carefully turn the palmrest over. Locate the cable harness which connects the glidepoint and speakers to the system. Disconnect the glidepoint and speaker cable harness from the palmrest/glidepoint assembly. You can now remove the palmrest/glidepoint assembly completely.
7. Lift up the front edge of the keyboard and fold it back carefully so that it is resting against the screen assembly.
8. Locate the audio connector board and the audio board that make up the audio card assembly. The connector board is secured by one screw at the front edge of the board. Remove this screw.
9. Two cable harnesses are connected to the audio board. One harness comes from the built-in microphone. The other harness connects to the built-in speakers. Remove both of these cable harnesses. The audio board is mated onto two connectors on the system motherboard carefully lever the audio board upwards until it disconnects from the motherboard. Slide the audio connector board out of the unit cabinet and remove the audio card assembly.
10. Locate the two ribbon cables that connect the rear edge of the keyboard to the system motherboard. The ribbon cables are held fast by locking connectors on the system motherboard. Unlock the cables by pulling upward on the motherboard connectors. Then remove the ribbon cables from the motherboard. You can now remove the keyboard completely.

C. Remove the CPU Module and the Power Module

1. Carry out all the steps of B. Remove the Palmrest/Glidepoint Assembly, the Keyboard, and the Audio Card Assembly.
2. Locate the power module. The power module is attached to the system motherboard by connectors at either end of the power module circuit board. Carefully lever the power module upwards until it disconnects from the motherboard.
3. Locate the CPU module. The CPU/Heat Sink Assembly module plugs directly into the system motherboard. Carefully lever the module upwards until it disconnects from the system motherboard.

D. Remove the Indicator Panel and Screen Assembly

1. Close the upper cover and turn the computer over. On the rear edge of the computer in the left and right corners, there are two screws, deeply recessed in the base of the unit. Remove these screws.
2. Turn the computer over and open the upper cover screen assembly to about 120 degrees. From the back of the computer, between the two screen hinges, use the two narrow openings to lever the back of the indicator panel upwards so that it disconnects from the base unit.
3. Carefully fold the indicator panel forwards. Locate the ribbon cable which connects the indicator panel to a locking connector on the VGA connector board. Pull the locking connector open and disengage the ribbon cable from the connector. You can then remove the indicator panel entirely.
4. Disconnect the two cable harnesses which connect the upper cover screen assembly to the VGA connector board. In addition, unscrew and release the two grounding cables which secure grounding wires from the upper cover screen assembly to the VGA connector board.
5. Straighten the upper cover screen assembly so that it is at an angle of 90 degrees to the base unit. Lift the upper cover directly upwards so that it disengages from the base unit.

E. Disassembly of the Base Unit Components

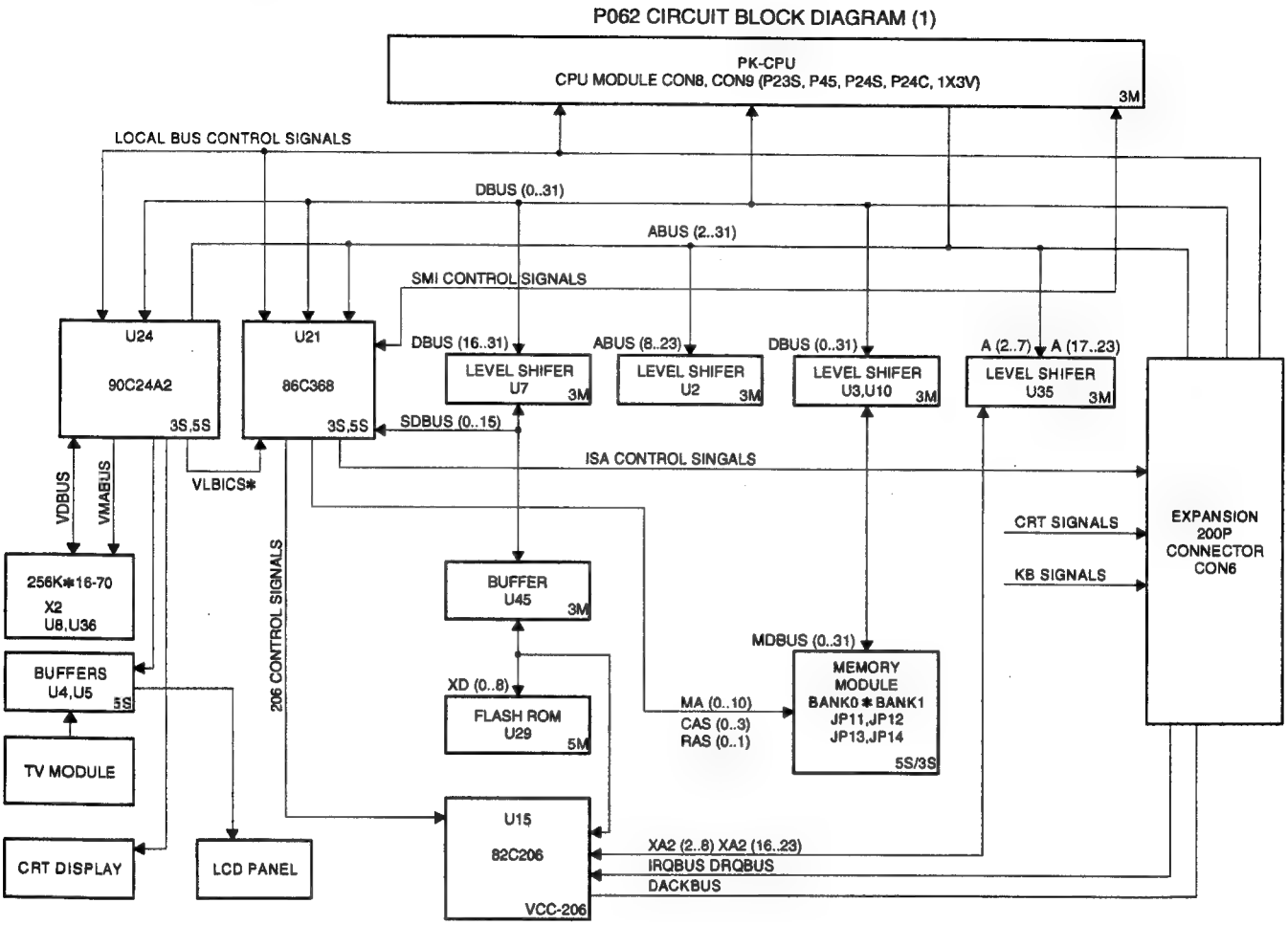
1. Remove the hard disk drive, and carry out steps B, C, and D described above.
2. Remove the upper frame from the base unit. The upper frame is held in position by plastic snap fasteners around the edge of the unit. Carefully loosen the upper frame and remove it from the base unit.
3. Remove the VGA connector board. The VGA connector board is held in place by two remaining screws on the rear edge at the right-hand and left-hand sides.
4. Disconnect the VGA connector board. A connector on the base of the VGA board is plugged into a connector on the system motherboard. Pull the board upwards to disconnect it. This requires some force.
5. Remove the battery bay and diskette drive shielding. Each shielding is held in place by two screws at the rear edge of the shielding. Remove the screws and then remove the shielding entirely.
6. Disconnect the cable harness from the GlidePoint which is still connected to the system motherboard.
7. Remove the system motherboard. The motherboard is held in place by two remaining screws. One screw is at the rear edge right corner, and the other screw is at the rear edge between the serial and PS/2 ports. Remove these screws.
8. Carefully remove the system motherboard from the base unit.

F. Complete Re-assembly of all components.

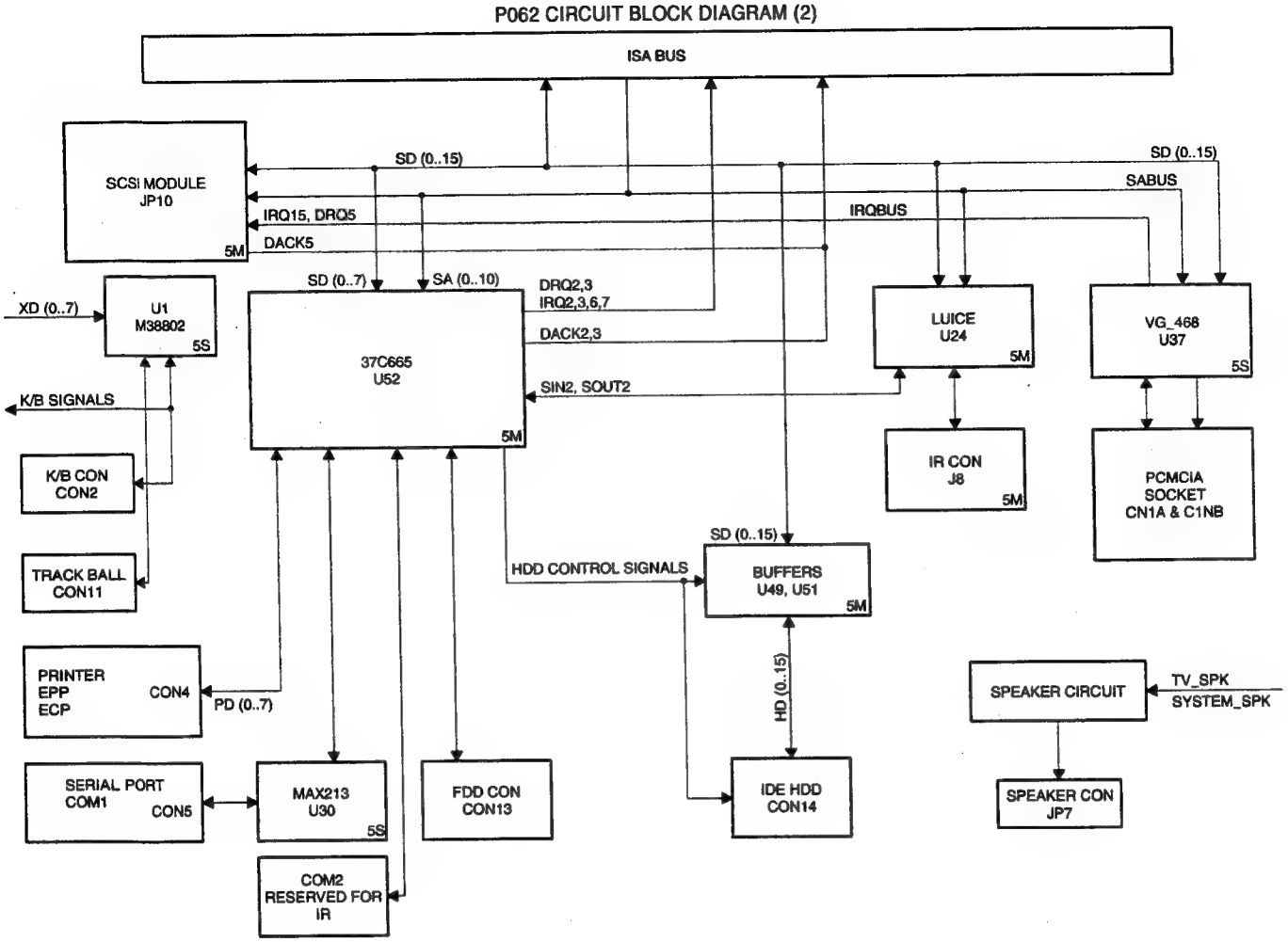
1. Place the system motherboard back into the base unit. Take care that in the rear right corner, the board does not interfere with the folded over guide for the screen assembly pin. Replace the screw in the rear right corner and the screw between the PS/2 and serial ports. Reconnect the GlidePoint cable harness to the system motherboard.
2. Replace the battery bay and diskette bay shielding and secure each into place with two screws.
3. At this point, you can re-install the CPU module and the power module, if they have been removed.
4. Re-install the VGA connector board. Secure it in place by replacing the two screws on the rear edge at the extreme left and right sides.
5. Re-install the upper frame of the base unit and press it into position so that the snap fasteners engage.
6. Re-install the upper cover screen assembly. Move the linking pins on the lower edge of the screen assembly so that they are pointing straight downwards. Hold the upper cover at an angle of 90 degrees to the base unit and lower the upper cover linking pins into the holes in the left and right rear corners of the base unit.
7. Push the upper cover back to about 120 degrees. Use two screws to reattach the grounding wires from the screen assembly to the VGA connector board. Reconnect the two cable harnesses from the screen assembly to the connectors on the VGA connector board.
8. Unlock the locking connector on the VGA connector board. Insert the ribbon cable from the indicator panel into the locking connector and lock it in place when it is fully inserted. Open up the screen cover until it is almost at 180 degrees. Place the indicator panel carefully back into place. Take care that the ribbon cable does not get snagged in when you press the indicator panel back in to the base unit. Pull the screen forward and install the back edge of the indicator panel first. Then move the screen back and snap the front edge of the indicator panel back into place.
9. Close the upper cover and turn the unit over. Replace the two screws into the recessed screw holes on the left and right corners of the rear edge of the base unit.
10. Turn the unit over and open up the screen assembly. Open up the locking connectors on the system motherboard. Hold the keyboard over the base unit and insert the two ribbon cables from the keyboard into the base unit. Press the locking connectors down to lock the cables into place.
11. Fold the keyboard back against the screen until the sound board has been installed. Install the sound board into the two connectors on the system motherboard. Install the sound connector board into the side of the cabinet and secure it in place with the single screw. Now reconnect the microphone cable harness and the speaker cable harness to the connectors on the sound board.
12. Fold the keyboard downwards and install it onto the base unit. Hold the palmrest and GlidePoint assembly over the base unit and reconnect the combined speaker and GlidePoint cable harness to the palmrest connector.
13. Re-install the palmrest and GlidePoint assembly into the base unit. Hold the palmrest and keyboard in place while you turn the unit over and secure the palmrest and keyboard by replacing the two screws in the battery bay and the two screws in the diskette drive bay.
14. Replace the hard disk drive, the diskette drive, and the battery.

CHAPTER 4. HARDWARE DESCRIPTION

1. Block Diagram

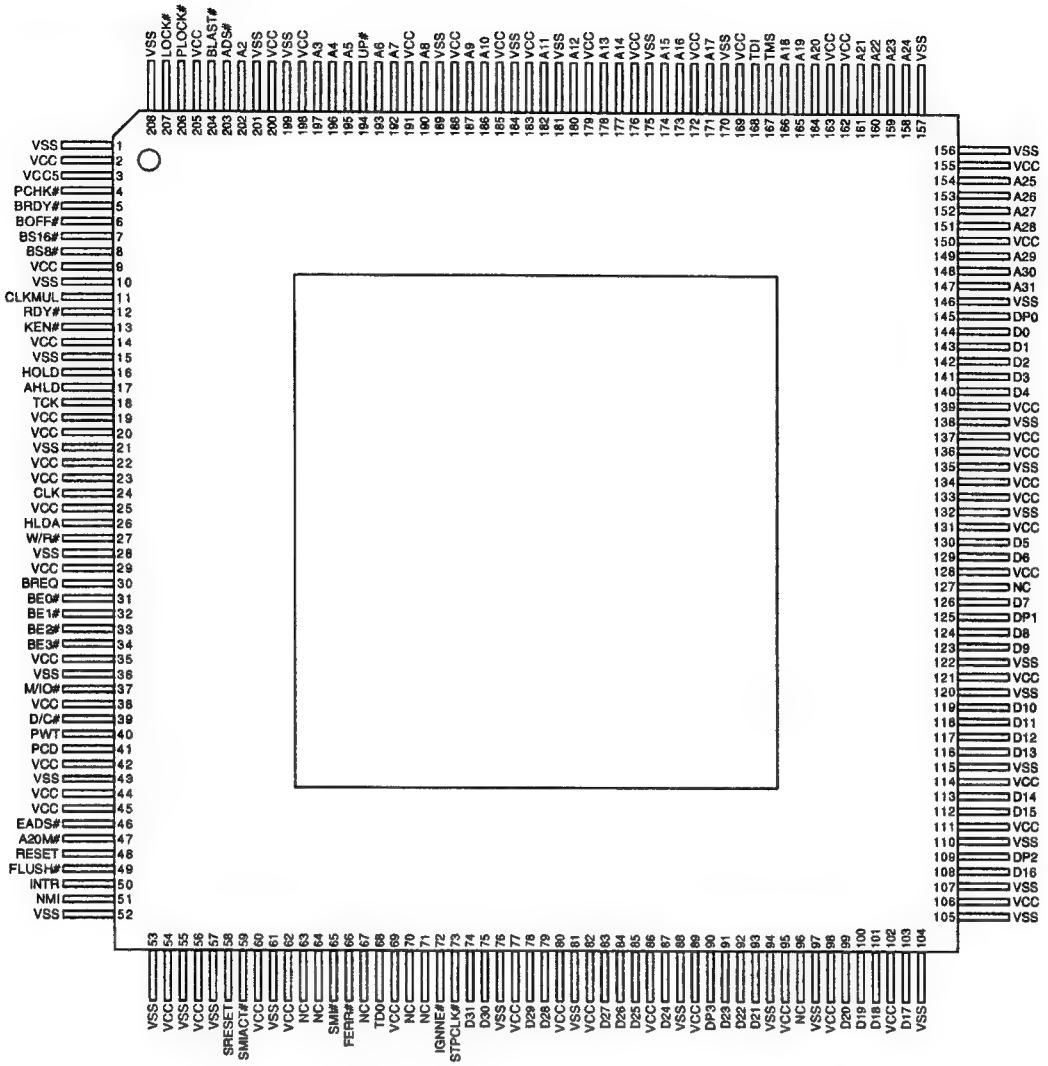


P062 CIRCUIT BLOCK DIAGRAM (2)



2. Intel SL-Enhanced

(1) Processor package diagram



208-Lead SQFP Pinout Diagram (Top View)

SQFP Package Pin List (Numerical Order)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	Vss	53	Vss	105	Vss	157	Vss
2	Vcc	54	Vcc	106	Vcc	158	A24
3	Vcc5	55	Vss	107	Vss	159	A23
4	PCHK#	56	Vcc	108	D16	160	A22
5	BRDY#	57	Vss	109	DP2	161	A21
6	BOFF#	58	SRESET	110	Vss	162	Vcc
7	BS16#	59	SMIACT#	111	Vcc	163	Vcc
8	BS8#	60	Vcc	112	D15	164	A20
9	Vcc	61	Vss	113	D14	165	A19
10	Vss	62	Vcc	114	Vcc	166	A18
11	CLKMUL	63	NC(1)	115	Vss	167	TMS
12	RDY#	64	NC(1)	116	D13	168	TDI
13	KEN#	65	SMI#	117	D12	169	Vcc
14	Vcc	66	FERR#	118	D11	170	Vss
15	Vss	67	NC(1)	119	D10	171	A17
16	HOLD	68	TDO	120	Vss	172	Vcc
17	AHOLD	69	Vcc	121	Vcc	173	A16
18	TCK	70	NC(1)	122	Vss	174	A15
19	Vcc	71	NC(1)	123	D9	175	Vss
20	Vcc	72	IGNNE#	124	D8	176	Vcc
21	Vss	73	STPCLK#	125	DP1	177	A14
22	Vcc	74	D31	126	D7	178	A13
23	Vcc	75	D30	127	NC(1)	179	Vcc
24	CLK	76	Vss	128	Vcc	180	A12
25	Vcc	77	Vcc	129	D6	181	Vss
26	HLDA	78	D29	130	D5	182	A11
27	W/R#	79	D28	131	Vcc	183	Vcc
28	Vss	80	Vcc	132	Vss	184	Vss
29	Vcc	81	Vss	133	Vcc	185	Vcc
30	BREQ	82	Vcc	134	Vcc	186	A10
31	BE0#	83	D27	135	Vss	187	A9
32	BE1#	84	D26	136	Vcc	188	Vcc
33	BE2#	85	D25	137	Vcc	189	Vss
34	BE3#	86	Vcc	138	Vss	190	A8
35	Vcc	87	D24	139	Vcc	191	Vcc
36	Vss	88	Vss	140	D4	192	A7
37	M/IO#	89	Vcc	141	D3	193	A6
38	Vcc	90	DP3	142	D2	194	UP#
39	D/C#	91	D23	143	D1	195	A5
40	PWT	92	D22	144	D0	196	A4
41	PCD	93	D21	145	DP0	197	A3
42	Vcc	94	Vss	146	Vss	198	Vcc
43	Vss	95	Vcc	147	A31	199	Vss
44	Vcc	96	NC(1)	148	A30	200	Vcc
45	Vcc	97	Vss	149	A29	201	Vss
46	EADS#	98	Vcc	150	Vcc	202	A2
47	A20M#	99	D20	151	A28	203	ADS#
48	RESET	100	D19	152	A27	204	BLAST#
49	FLUSH#	101	D18	153	A26	205	Vcc
50	INTR	102	Vcc	154	A25	206	PLOCK#
51	NMI	103	D17	155	Vcc	207	LOCK#
52	Vss	104	VSS	156	Vss	208	Vss

NOTE: 1. Pins listed as "NC" should always remain unconnected.

IntelDX4™ Processor Output Pins

Name	Active Level	When Floated
BREQ	HIGH	
HLDA	HIGH	
BE3# ~ BE0#	LOW	Bus Hold
PWT, PCD	HIGH	Bus Hold
W/R#, M/IO#, D/C#	N/A	Bus Hold
LOCK#	LOW	Bus Hold
PLOCK#	LOW	Bus Hold
ADS#	LOW	Bus Hold
BLAST#	LOW	Bus Hold
PCHK#	LOW	
FERR#	LOW	
A3 ~ A2	N/A	Bus Hold Address Hold
SMIACT#	LOW	
VOLDET	LOW	
TDO	N/A	

IntelDX4™ Processor Input/Output Pins

Name	Active Level	When Floated
D31 ~ D0	N/A	Bus Hold
DP3 ~ DP0	HIGH	Bus Hold
A31 ~ A4	N/A	Bus Hold Address Hold

NOTE: All outputs and I/O's except VOLDET are floated when UP# is asserted.

IntelDX4™ Processor Input Pins

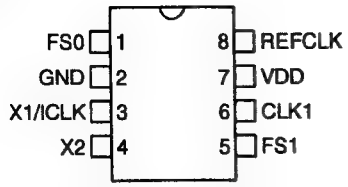
Name	Active Level	Synchronous/ Asynchronous	Internal Pull-Up/ Pull-Down
CLK	N/A		
RESET	HIGH	Asynchronous	
SRESET	HIGH	Asynchronous	Pull-Down
HOLD	HIGH	Synchronous	
AHOLD	HIGH	Synchronous	Pull-Down
EADS#	LOW	Synchronous	Pull-Up
BOFF#	LOW	Synchronous	Pull-Up
FLUSH#	LOW	Asynchronous	Pull-Up
A20M#	LOW	Asynchronous	Pull-Up
BS8#/BS16#	LOW	Synchronous	Pull-Up
KEN#	LOW	Synchronous	Pull-Up
RDY#	LOW	Synchronous	
BRDY#	LOW	Synchronous	Pull-Up
INTR	HIGH	Asynchronous	
NMI	HIGH	Asynchronous	
IGNNE#	LOW	Asynchronous	Pull-Up
SMI#	LOW	Asynchronous	Pull-Up
STPCLK#	LOW	Asynchronous	Pull-Up
UP#	LOW		Pull-Up
CLKMUL	N/A		Pull-Up
TCK	N/A		Pull-Up
TDI	N/A		Pull-Up
TMS	N/A		Pull-Up

IntelDX4™ Processor Test Pins

Name	Input or Output	Sampled/Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Falling Edge of TCK
TMS	Input	Rising Edge of TCK

3. AV9107-05 Clock Generator

Pin Configurations



AV9107-05
8pin DIP, SOIC

AV9107

Decoding Table for AV9107-05, 14.318 input

FS1	FS0	CLK1
0	0	40 MHz
0	1	50 MHz
1	0	66.6 MHz
1	1	80 MHz

Decoding Table for AV9107-03, 14.318 input

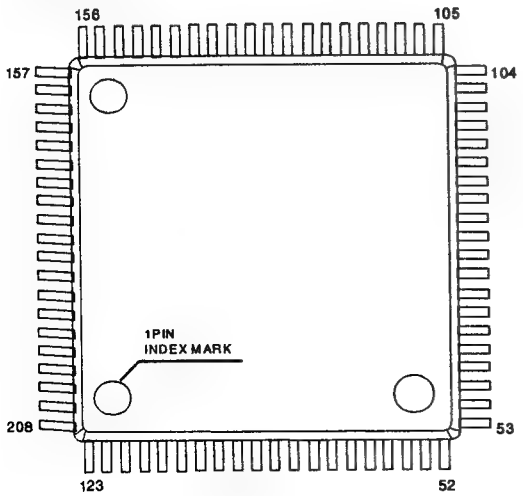
FS3	FS2	FS1	FS0	CLK1
0	0	0	0	16 MHz
0	0	0	1	40 MHz
0	0	1	0	50 MHz
0	0	1	1	80 MHz
0	1	0	0	66.66 MHz
0	1	0	1	100 MHz
0	1	1	0	8 MHz
0	1	1	1	4 MHz
1	0	0	0	8 MHz
1	0	0	1	20 MHz
1	0	1	0	25 MHz
1	0	1	1	40 MHz
1	1	0	0	33.33 MHz
1	1	0	1	50 MHz
1	1	1	0	4 MHz
1	1	1	1	2 MHz

Pin Description for AV9107-03, AV9107-05

Pin Name	Pin #		Pin Type	Description
	-05	-03		
FS0	1	14	Input	FREQUENCY SELECT 0 for CLK1 (-03 has pull-up)
FS1	5	1	Input	FREQUENCY SELECT 1 for CLK1 (-03 has pull-up)
FS2		2	Input	FREQUENCY SELECT 2 for CLK1 (-03 has pull-up)
FS3		3	Input	FREQUENCY SELECT 3 for CLK1 (-03 has pull-up)
AGND		4	—	Analog GROUND
GND	2	5	—	Digital GROUND
PD*		6	Input	POWER DOWN. Shuts off chip when low. Internal pull-up
X1/ICLK	3	7	Input	CRYSTAL INPUT or INPUT CLOCK frequency. Typically 14.318 MHz system clock
X2	4	8	Output	CRYSTAL OUTPUT (No Connect when clock used)
OE(REFCLK)		9	Input	OUTPUT ENABLE. Tri-states REFCLK when low. Pull-up
OE(CLK1)		10	Input	OUTPUT ENABLE. Tri-states CLK1 when low. Pull-up
CLK1	6	11	Output	CLOCK1 Output (see decoding tables)
VDD	7	12	—	Digital power supply (+5V DC)
REFCLK	8	13	Output	REFERENCE CLOCK output. Produces a buffered version of the input clock or crystal frequency (typically 14.318 MHz)

4. Pico Power Pt86C368 AT Chipset

(1) Pin Diagram



PT86C268 Pin Diagram

(2) Pin Description

Clock and Reset Interface

Pin Name	I/O	Pin Description	Pin#
CLK2IN	I	2X Clock Input: This input clock must be two times the CPU clock speed with a 50/50 duty cycle.	42
CPUCLK	I/O 8mA	CPU Clock Output: This will be either a 1X or a 2X clock output for a 486 CPU, or a 2X clock output for the a 386 CPU as determined by an RC-RESET option select.	109
CLKSEL (BUSTYI)	I/O 2mA	Clock Select: This output selects the 2X clock source option on the Intel 486LP CPU's. This pin is also used as BUSYI input from 387 in 386DX mode.	164
SCLK206	O 2mA	System Clock 206: This is an approximately 8MHz output to the Timer in the 82C206 Peripheral Controller.	124
TMRCLK	O 2mA	Timer Clock: This output is a 1.2MHz clock used to drive the timer in the 82C206 Peripheral Controller.	126
$\overline{\text{RCRST}}$	I	$\overline{\text{RC-RESET}}$: This input is used to reset the Evergreen HV's Power Management Controller upon initial system power-up. It should have a pull-up resistor ried to the same power source as the Evergreen HV.	162
PWRGOOD	I	Power Good Input: This input causes a complete system reset when it is drive low by the PWRGOOD signal from the power supply or a reset switch.	139
RSTDRV	O 12mA	AT Bus Reset Output: This output provides a system reset to the AT Bus and Peripherals.	97
RSTCPU	O 2mA	CPU Reset Output: This is the reset output to the CPU	185
SPNDNRST	O 2mA	Suspend Not Reset: This output provides a reset equivalent to RSTDRV except when in suspend mode. Any device not powered down during suspend mode should use this reset.	55

CPU Interface

Pin Name	I/O	Pin Description	Pin#
A<31.26:24, 16:2>	I/O 4mA	CPU Addresses. A<31.26:24.16:2>: These ars address inputs from the CPU. These pins also output DMA and Refresh addresses.	5.4-2 202-192179 -176
A<23:17	I	CPU Addresses. A<23:17>: These are address inputs irom the CPU .	I. 208-203
$\overline{\text{BE<3:0>}}$	I	CPU Byte Enables <0.3>#: These inputs from the CPU control selection of individual bytes of data.	13-10
D<15:0>	I/O 4mA	CPU Data <15:0>: These are the low word of CPU data.	29-16 184.183
$\overline{\text{ADS}}$	I	$\overline{\text{Address Status}}$: This input from the CPU indicates the presentation of a valid address and cycle definition from the CPU.	188
$\overline{\text{(SMIACT)}}$ $\overline{\text{(SMIADS)}}$	I I	*$\overline{\text{System Management interrupt Active Status}}$: This input from some CPU's indicates that an SMI routine is in progress.* System Management Interrupt Address Starus#: This input indicates the presentation of a valid SMI address and cycle detinition on some CPU's.	187
$\overline{\text{W/R}}$	I	Write/read #: This Input From the CPU Indicates Whether the Current Cycle is a Write or Read Access.	7
$\overline{\text{D/C}}$	I	$\overline{\text{Data/Code}}$: This Input From the CPU Indicates Whether the Current Cycle is a Data or Code access.	9

Pin Name	I/O	Pin Description	Pin#
M/IO	I	$\overline{\text{Memory/IO}}$: This Input From the CPU Indicates Whether the Current Cycle is a Memory or I/O access.	8
$\overline{\text{(EADS)}}$ $\overline{\text{(ERRORO)}}$	O 2mA	$\overline{\text{External Address Valid}}$: This Output to the 486 CPU indicates thst a valid address has been drive onto the CPU address bus which the 486 will use for an internal cache invalidation cycle.	34

Pin Name	I/O	Pin Description	Pin#
$\overline{\text{RDY}}$	/O 4mA	$\overline{\text{Read}}$: This output to the CPU indicates completion of the current bus cycle. This pin is also an input to monitor completion of local bus cycles.	15
$\overline{\text{(BRDY)}}$ (PEREQO)	/O I4mA	$\overline{\text{Burst Ready}}$: This output to the 486 CPU indicates completion of the current access and indicates that the CPU may burst the subsequent access. This pin is also an input to monitor completion of local bus cycles.	14
$\overline{\text{(BLAST)}}$ (PEREQI)	I	$\overline{\text{Bures Last}}$: This input from the 486 CPU Indicates thst next BRDY# will complete the current burst cycle.	186
$\overline{\text{(FERR)}}$ $\overline{\text{(ERRORI)}}$	I	$\overline{\text{Floating Point Error}}$: This input from the 486DX CPU indiccates a 486DX internal floating point error.	33

Pin Name	I/O	Pin Description	Pin#
(IGNNE) (BUSYO)	O 2mA	Ignore Numeric Error : This output to the 486DX CPU indicates thst floation point errors should be ignored.	36
KEN) (RSTNPU)	O 2mA	Cache Enable : This outputto the 486 CPU indicates that the current bus cycle in cacheable.	30
NMI	O 2mA	Non Maskable Interrupt: This output to the CPU indicates the occurrence of a Non Maskable Interrupt.	35
A20M	O 2mA	Address Bit 20 Mask : This output to the 486 CPU indicates thst the CPU should nask A20 in order to emulate the 8086 address wrap around.	32
HOLD	O 2mA	Hold Request: This output to the CPU indicates a request to hold the Request.	6
SRESET) (SMIRDY) (GPOB0)	O 4mA	*Soft reset : This output to some CPU's indicates a software generated CPU reset request.* System Management Interrupt Ready #: For some CPU's this output indicates completion of an SMI bus cycle. General Purpose Output B0: if not used for either of the orther optionnal functions this pin may be used as a GPO. Please see configuration register 18 for specific details.	181
(STPCLK) (IIBEN) (GPOBI)	O 4mA	*Soft reset : For some CPU's this output to the CPU toindicates a stop clock request.* I/O Instruction Break Enable #: This output drives the IIBEN# input of some CPU's. General Purpose Output BI: if not used for either of the orther optional functions this pin may be used as a GPO. Please see configuration register 18 for spacific details.	182
LOCAL	i	Local Device : This input from a local bus device indicates that tha local device has claimed the current CPU cycle and it should therefore be ignored by the Evvergreen HV.	37

DRAM Interface

Pin Name	I/O	Pin Description	Pin#
DRAMW	O 12mA	DRAM Write Enable : This output drives Write Enable for all DRAM's.	175
RAS<3.0>	O 12mA	Row Address Strrobes <3.0>: These output drive the RAS# inputs on DRAM banks 3 to 0.	4777
CAS<3:0>	O 12mA	Column Address Strobes <3.0> : These output drive the RAS# inputs on DRAM bytes 3 to 0.	169, 168, 166.52
MA<10:0>	I/O 12mA	Memory Address <10:0> These output drive the MA Lines for all DRAM's They are also used as RC-RESET configuration inputs during power up.	174-171, 5148, 40-38

Peripheral Controller Interface

Pin Name	I/O	Pin description	Pin#
ASRTC	O 2mA	Address Strobe for Real Time Clock: This output Drives the Address Styobe of the 82C206's internal Real Time Clock.	130
HRQ	I	Hold Request: This input from the 82X206 indicates a request to hold the CPU and float its bus.	132
HLDA206	O 2mA	Hold Acknowledge 206: This output drives the HLDA input of the 82C206.	133
INTR	I	Interrupt Request: This input from the 82C206 indicates an interrupt reqest to the CPU.	129
INTA	O 2mA	Interrupt Acknowledge : This output to the 82C206 indicates an Interrupt Acknowlege from the CPU.	116
GATE2	O 2mA	GATE 2: This output drives the GATE2 input of the 82C206's internal Timer 2.	119
OUT2	I	OUT 2: This input is driven from the 82C206's internal Timer 2 Output.	117
ADSTB8	I	Address Strobe 8 bit; This input from the 82C206 indicates an 8 bit DMA Address.	128
ADSTB16	I	Address Strobe 16 bit: This input from the 82C206 indicates an 16 bit DMA Address.	127
IRQ13	O 2mA	Interrupt Request 13: This input from the 82C206 Peripheral Controller indicates a numeric coprocessor interrupt request.	123
REFREQ	I	Refresh Requset: This input from the 82C206 Peripheral Controller indicates a refresh request.	118
AEN8	I	Address Enable 8 bit : This input indicates an 8 bit DMA Cycle.	120
AEN16	I	Address Enable 16 bit: This input indicates an 16 bit DMA Cycle.	121
AEN206	O 2mA	Address Enable 82C206 : This output drives the 82C206's ACK input.	134

AT Bus Interface

Pin Name	I/O	Pin Description	Pin#
SA<7.0>	O 12mA	Slot Addresses<7:2>: These outputs are buffered from the equivalent CPU addresses to drive the SA Bus.	69-71 , 73. 92, 93
SA<1:0>	O 12mA	Slot Addresses <1.0>: These outputs are decoded from the CPU byte enables to drive these AT Bus address lines.	95, 96
SD<15.0>	O 12mA	Slot Data<15:0>:These I/O are the data read and write path for the AT Bus.	110, 111. 113, 114. 75-77. 79, 84-67. 87-90
BALE	O 12mA	Buffered Address Latch Enable: This output is driven to the AT Bus where it indicates the presence of a valid address on the Bus.	109
MASTER	I	Master : This input from the AT Bus indicates thst a slot master has take control of the AT Bus.	105

Pin Name	I/O	Pin Description	Pin#
$\overline{\text{MEMR}}$	O 8mA	$\overline{\text{Memory Read}}$: This output to the AT Bus indicates a Memory Read cycle to any valid AT Bua address. This pin aslo acts as an input to provide for MASTER access to local DRAM.	100
$\overline{\text{MEMW}}$	O 8mA	$\overline{\text{Memory Write}}$: This output to the AT Bus indicates a Memory Write cycle to any valid AT Bua address. This pin aslo acts as an input to provide for MASTER access to local DRAM.	102
$\overline{\text{SMEMR}}$	O 12mA	$\overline{\text{Slot Memory Read}}$: This output to the AT Bus indicates a Memory Read cycle within the 0 to IMB address range.	86
$\overline{\text{SMEMW}}$	O 12mA	$\overline{\text{Slot Memory Write}}$: This output to the AT Bus indicates a Memory Write cycle within the 0 to IMB address range.	85
$\overline{\text{IOR}}$	O 12mA	$\overline{\text{I/O Read}}$: This output to the AT Bus indicates an I/O Read cycle.	99
$\overline{\text{IOW}}$	O 12mA	$\overline{\text{I/O Write}}$: This output to the AT Bus indicates an I/O Write cycle.	98
$\overline{\text{MEMCS16}}$	I	Memory Chip Select 16 Bit #: This input from the AT Bus indicates that the current access is to a 16 bit memory device.	103
$\overline{\text{IOC16}}$	O 8mA	$\overline{\text{I/O Chip Select 16 bit}}$: This impuy from the AT Bus indicates that the current access is to a 16 bit I/O device.	108
$\overline{\text{SBHE}}$	O 12mA	$\overline{\text{Slot Byte High Enable}}$: This output to the AT Bus indicates a data transter on the high byte of the Slot Data Bus.	115
$\overline{\text{IOCHCK}}$	I	$\overline{\text{I/O Channel Check}}$: This input indicates a parity error from some device on the AT Bus.	81
IOCHRDY	I	I/O Channel Read: When this input is driven low it indicates thst the deviceon AT Bus currently being accessed requirs additional time to complete the cucle.	80
$\overline{\text{ZWS}}$	I	$\overline{\text{Zero Wait State}}$: This input from the AT Bus indicates that the device currently bring accessed can complete the cycle with zero wait stares.	74
TURBOBUS	O 12mA	TurboBus: This output is driven high on TurboBus cycles in order to shield the AT Bus from substandard commend strobes.	131
SYSCLK	O 12mA	System Clock: This output to the AT Bus provides an approximate 8MHz clock.	82

Pin Name	I/O	Pin Description	Pin#
AEN	O 12mA	Address Enable: This output to the AT Bua indicates that the DMA conntroller has taken control of the CPU address bus and the AT Bus command lines.	104
$\overline{\text{REFRESH}}$	O 12mA	$\overline{\text{Refresh}}$: This output drives the AT Bus to indicates a Memory Reiresh Cycle.	107

Buffer control

Pin Name	I/O	Pin Description	Pin#
SDDIR	O 2mA	Slot Data Driection: This output drices the DIR control of the D<31:16>to SD<15:0> transceiver.	157
$\overline{\text{SDEN2}}$	O 2mA	$\overline{\text{Slot Data Enable 2}}$: This output drices the G# of the D<23:16>to SD<7:0> transceiver.	158
$\overline{\text{SDEN3}}$	O 2mA	$\overline{\text{Slot Data Enable 3}}$: This output drices the G# of the D<31:24>to SD<15:8> transceiver.	159
XDDIR	O 2mA	Extended Data Direction: This output drives the DIR controlof the optional XD to SD transceiver.	138
MDDIR (GPIOAI) (ELB1)	I/O 2mA	Buffer Direction : This output drives the DIR input of the optional D to MD transceiver. This pin may also be used as an optional GPIO. Please see configuration register 18 for specific details.	165
$\overline{\text{MDEN}}$ (GPIOAI) (ELB1)	I/O 4mA	Buffer Enable : This output drives the G# input of the optional D to MD transceivers. This pin may also be used as an optional GPIO. or an Extended Low Battery Detecl. Please see configuration register 18H for specific details.	160

Power Management Interface

Pin Name	I/O	Pin Description	Pin#
32KIN	I	32KHL Input: This input is used to count the refresh interval during Suspend Mode.	153
14MHZIH	I	14.318 Mega Hertz Input: This input is used to generate the timer clock for the 82C206 Peripheral Controller.	122
(KBCLKI) (GPIOC0)	I/O 4mA	Keyboard Clock Input: This input generate the Keyboard Clock Output. This pin may also be used as an optional GPIO. Please see register section 10.4.18 for specific details.	57
(KBCLKO) (GPIOC0)	I/O 4mA	Keyboard Clock Output: This output drives the Keyboard Controller clock input. This pin may also be used as an optional GPIO. Please see register section 10.4.18 for specific details.	58

Pin Name	I/O	Pin Description	Pin#
(PMI) (IRQX) (SMI)	I/O 4mA	Power Management Interrupt: This output indicates a power manegement interrupt. It should be connrcted to either IRQX for a Non-SMI CPU or to SMI for any SMI compatible CPU.	180
PC<4:0>	O 2mA	Power Control<4:0>:These output provides inividual power control for five system components.	146-142
(PC<5>) (LEDFLSH)	O 2mA	Power Control<5>: This Output provides individual power contril for one system component. LED Flacher: This output can optionally be used to control one or more flashing LED's to indicate verious system status conditions such as Low Battery or Suspend Mode. Please see register section 6.5 for more details.	147
PC<6>	O 2mA	Power Control<6>: This Output provides individual power contril for one system component.	148
PC<7>	O 2mA	Power Control<7>: This Output provides individual power contril for one system component.	149
PC<8>	O 2mA	Power Control<8>: This Output provides individual power contril for one system component.	150
(PC9) (PCBKLT)	O 2mA	Power Control<8>: This Output provides an individual power contril for one system component. Power Control for Backlight: This ouyput can optionally be controlled directly by the peripheral/backlight timer.	151
DPIO <3.0>	I/O 4mA	General purpose I/O's <3:0>: These four I/O's are provided for general purpose usage.	54.53 156. 155
RING	I	Ring: This input provides for a "wake-up" call from a modem.	152
SWTCH	I	Switch: This input provides an on-off function between Fully-On and Standby Modes.	140
EXTACT	I	External Activity: This input indicates thst there is current external activity.	161

Battery Manegement Interface

Pin Name	I/O	Pin Description	Pin#
ACPWR	I	AC Power: This input indicates that the current power source is AC.	135
LB	I	Low Battery: This input from the power supply indicates a low battery condition.	136
VLB	I	Very Low Battery: This input from the power supply indicates a very low battery condition.	137

System Miscellaneous

Pin Name	I/O	Pin Description	Pin#
$\overline{\text{KBDCCS}}$	I/O	Keyboard Controller Chip Select #: This ouypuy drives the 8042, or equivalent, Keyboard Controller Chip Select.	59
$\overline{\text{ROMCS}}$	O 2mA	ROM Chip Select #: This output drives the BIOS ROM Chip Select.	60
SPKR	O 2mA	Speaker: This output drives the system apeaker.	63
VDDCL <1:0>	--	Core Logic Power Pins	61, 141
VSSCL <0:1>	--	Core Logic Power Pins	163, 83
VDDIO <9:0>	--	I/O Power Pins	43, 167. 191. 62. 68. 78. 91. 101. 112. 154
NSSIO <8:0>	--	I/O Ground Pins	41. 56. 72. 84. 94. 106. 125. 170. 189.

Muliti-Function NPU Pins

The interface control signals between a 386DX and a 387 NPU are significantly different from those used in a 486 system. In order to save pins these seversl signals unique to 386 implementation are shared with several signals uniqur to the 486. The following table indicates which pins are shared and described the 386 function of each.

Multi-function Pins -- 486 vs 386DX

486 NAME	386 NAME	I/O	386 DESCRIPTION	PAD I/O
$\overline{\text{EADS}}$	$\overline{\text{ERRORO}}$	O	Error output: This pin is the moditied ERROR output to the 386DX.	O
$\overline{\text{BLAST}}$	PEREQI	I	Processor Extension Request Input: This input from a 387 indicates an NPU cycle request.	I
$\overline{\text{BRDY}}$	PEREQO	O	Processor Extension Request Output: This output from a 387 indicates an NPU cycle request.	O
$\overline{\text{FERR}}$	$\overline{\text{ERRORI}}$	I	Error Input: Thispin is the ERROR input from a 387 NPU.	I
$\overline{\text{IGNNE}}$	$\overline{\text{BUSYO}}$	O	Busy Output: This output to a 386DX indicates that the NPU is executing NPU cycles.	O
$\overline{\text{KEN}}$	RSTNPU	O	Reset NPU: This output signals a reset for a 387 NPU.	O
CLKSEL	$\overline{\text{BUSYI}}$	I	Busy Input: This input from the a 387 NPU indicates that it is executing NPU cycleS.	I/O

5. Memory Controller

5-1. Description

The PT86C368 implements a high performance Burst Mode DRAM Controller for optimal 486 system performance.
In addition to the Burst Mode capability, the PT86C368 also incorporates Page Mode operation. This takes advantage of the DRAM's built in Page Mode feature to allow faster memory accesses within a selected row--also known as a page.
The memory capacity of the PT86C368 is up to four banks and 64M bytes of local DRAM. The maximum memory size would be achieved by installing 4 banks of 4M DRAM's which provide 16M bytes per 32 bit bank for a total of 64M. In addition the four bank capability is very useful with lower density DRAM's such as the 256K and 512K which provide 1M and 2M per 32 bit bank respectively.
The PT86C368 provides unlimited flexibility by allowing virtually any combination of standard DRAM's. The basic memory types supported are, 256K x4, 256K x 16, 512K x 8, 1M x 1, 1M x 4, 4M x 1, and 4M x 4. The Evergreen HV provides unlimited flexiblity of installation by allowing the manufacturer or user to plug in any combination of different DRAM types in any order. And the entire memory configuration procedure can be handled automatically by a simple BIOS routine.

5-2. DRAM Timing Control

1. DRAM Timing Programmability

IN order to allow the system designer to best optimize for their specific system configurations, the PT86C268 DRAM Controller has included programmable options for several of the most critical DRAM timing parameters. Following are brief descriptions of the programmable options.
RAS Precharge: The RAS Precharge time for a page miss cycle can be programmed to either 0 or 1 wait state. With 0 wait states the RAS precharge time will be 2.5 CLK2's. And with I wait state the RAS precharge time will be 4.5 CLK2's.
RAS Precharge Stretch: For some conditions the RAS Precharge may not need a full wait state. In these cases the RAS Precharge can be programmed for a half clock stretch which will improve pertormance and save power. With the half clock stretch the RAS precharge time will be 3.5 CLK2's.
CAS Precharge: The Read-CAS Precharge time should be set to 0.5 CLK2's when the Read-CAS Pulse Width is programmed to 0 wait states, and it should be set to 1 CLK2 when the Read-CAS Pulse Width is programmed to I wait state.
Read-CAS Pulse Width: The Read-CAS Pulse Width can be programmed to either 0 or 1 wait states. With 0 wait states the Read-CAS Pulse Width will be 1.5 CLK2's. And with 1 wait state the Read-CAS Pulse
Width time will be 3 CLK2's.
Read-CAS Stretch: For some conditions the Read-CAS pulse width may not need a full wait state. In these cases the Read-CAS can be programmed for a half clock stretch which will improve performance and
save power. With the half clock stretch the Read-CAS Pulse Width will be 2.5 CLK2's.
Write-CAS Pulse Width: The Write-CAS Pulse Width can be programmed to either 0 or 1 wait states. With 0 wait states the Write-CAS Pulse Width will be 1 CLK2. And with 1 wait state the Write-CAS Pulse Width time will be 2 CLK2's.
Please see register sections 10.3.2-3 for specific details on the programming of DRAM timings.

2. Automatic Page Sizing

The minimum page size for each bank of DRAM is determined by the smallest type of DRAM installed, with the default being 2KB per page. With 256K or 512K memory installed the page size will always be limited to 2K. However, if the minimum memory size installed is M or 4M then the page size can be increased to 4KB or 8KB respectively. This page resizing can also be done automatically by the BIOS at the same time that it evaluates memory types and calculates starting addresses. The advantage of the larger page sizes is a slightly higher hit rate for the page mode DRAM Controller.

Minimum Page Size = 2KB											
MA	10	9	8	7	6	5	4	3	2	1	0
RAS	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
CAS	A23	A21	A10	A9	A8	A7	A6	A5	A4	A3	A2

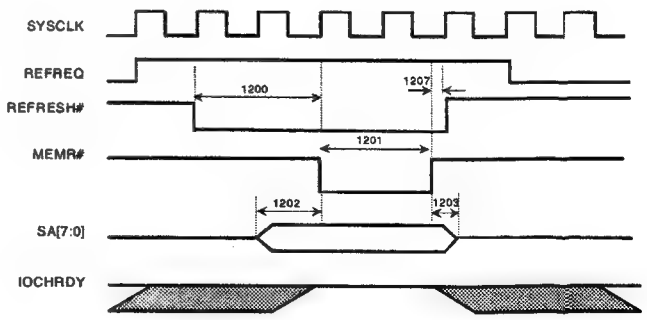
Minimum Page Size = 4KB											
MA	10	9	8	7	6	5	4	3	2	1	0
RAS	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
CAS	A23	A21	A10	A9	A8	A7	A6	A5	A4	A3	A2

Minimum Page Size = 8 KB											
MA	10	9	8	7	6	5	4	3	2	1	0
RAS	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
CAS	A23	A21	A10	A9	A8	A7	A6	A5	A4	A3	A2

5-3. Refresh Controll

1. Hidden AT Bus Refresh

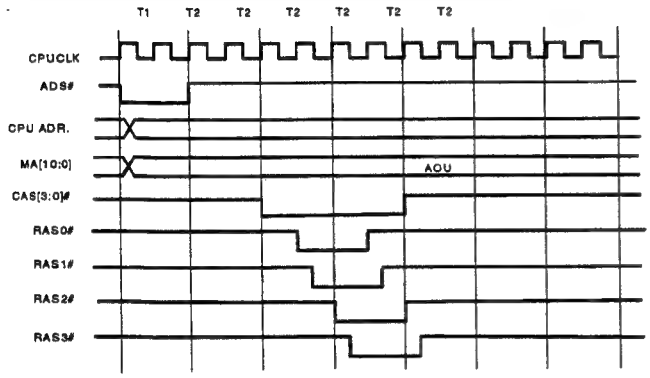
The PT86C368 implements a hidden AT Bus refresh mechanism. This hidden refresh works by decoupling the AT Bus from the CPU Bus and from local memory, such that AT Bus refresh cycles may occur simultaneously with CPU accesses to local memory. The result is that AT Bus refresh cycles no longer hold up the CPU since they occur in parallel with normal CPU operation. This parallelism provides a significant increase in system performance, typically on the order of 5%. The 5% savings is directly attributable to the amount of time normally used up by the AT Bus refresh cycle due to its slow
clock and the associated hold synchronization time. And although the AT Bus refresh is hidden, its operation on the bus is still completely AT compatible, including the standard AT refresh counter and RAS-only refresh control logic.



AT Bus Refresh Timing

2. Staggered CAS Before RAS Refresh of Local DRAM

CAS before RAS refresh is provided for local DRAM under periodic control of either system timer two or the dedicated Evergreen HV refresh timer. CAS before RAS is a very efficient refresh method in that it utilizes refresh address counters internal to the DRAM. This means that a refresh address need not be driven from the Evergreen HV, only the CAS and RAS lines are asserted. In addition the RAS lines are staggered in time to minimize the associated power surge. Further, since the local memory refresh is completely decoupled from the AT Bus refresh, the local memory can always use the slow refresh option.



Local DRAM Refresh in CPU Mode

5-4. Shadow RAM Control

The shadow RAW feature provides significant preformance enhancement on BIOS accesses. This feature is used by first copying the contents of any shadowable ROM from the ROM itself to DRAM located at the same address space. The transfer is made by first enabling the appropriate address space to the ROM Read/DRAM Write Mode. When enabled this mode provides that each memory read access is directed to the ROM and each memory write access is directed to the DRAM, such that each address can be read and immediately written back to perform the transfer. Once the transfer is complete the ROM has been "shadowed" in DRAM and the appropriate region of address space should then be set to the DRAM Read Only Mode. The entire BIOS region from C0000 to FFFFF is shadowable in the following increments.

Address Range	Segments	Block Size
F0000 to FFFFF	1	64K
C0000 to EFFFF	12	16K

5-5. ROM

1. Single 8 Bit BIOS ROM

The PT86C368 provides for a single 8 bit BIOS ROM in order to save both space and power. All necessary cycle conversion from 16 to 8 bit cycles is handled internally by the AT Bus Controller to provide the simplest possible BIOS ROM interface. This cycle conversion process takes longer to access the ROM since it converts one 16 bit cycle into two 8 bit cycles but this should not impact system performance since the BIOS ROM will typically be shadowed during system initialization.

2. Combined System & Video BIOS ROM

In order to provide the optimum in space and power savings, the PT86C368 provides the option of combining the system and video BIOS's into a single ROM. This option combined with the single 8 Bit BIOS ROM reduces the total ROM count from three for a typical AT system to only one for an Evergreen HV Portable.

3. Flash ROM Support

The Evergreen HV provides support for Flash ROM's through conditional control of the ROM$\overline{CS}$ pin. The FLASHENB bit in register 300H enables a Flash ROM to be written by providing a valid ROM chip select for any memory write to the ROM address range. Normally ROM$\overline{CS}$ would only be active on memory reads. When FLASHENB is low ROM$\overline{CS}$ will only respond to memory reads. With this implementation, the $\overline{MEMW}$ command can be directly connected to the program pin on the Flash ROM. Writes will only be effective, however, when the ROM$\overline{CS}$ is valid which means only when the FLASHENB bit is set high.

5-6. AT Bus Controller

The AT Bus Controller handles all operations to the AT Bus. This inciudes the monitoring of $\overline{IOCS16}$ and MEM$\overline{CS16}$ to determine byte or word data size, the monitoring of IOCHRDY and $\overline{ZWS}$ to determine appropriate cycle length, and as weill it includes the management of all data direction and drive controls. In addition the AT Bus Controller handles all cycle conversion requirements. These include conversion from double-word cycles to word or byte cycles and word to byte conversion as required by word or byte devices.

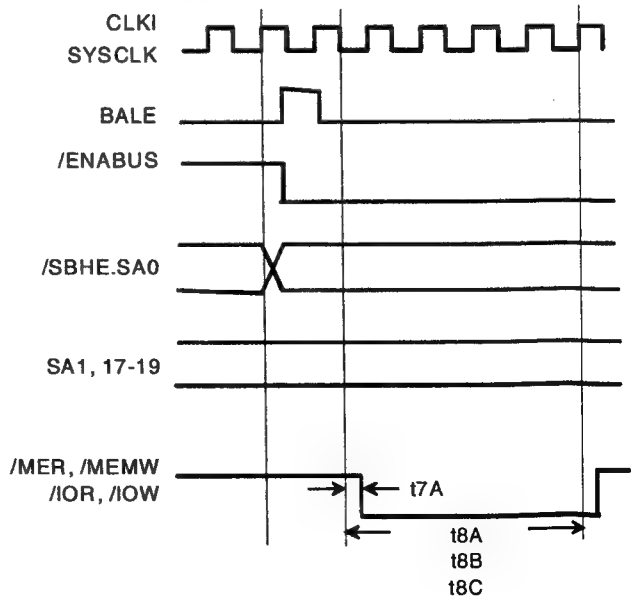
1. Quiet Bus

The Evergreen HV implements a Quiet Bus whereby none of the AT Bus signals will be driven by the Evergreen HV except during cycles that are specifically directed to the AT Bus. This restriction provides two advantages. First, this prevents slow devices on the AT Bus from being confused by the substandard pulse widths created by non-AT Bus cycles that run at higher speeds. And second, this feature also helps to reduce power consumption by avoiding the conventionally wasteful routine of needlessiy charging and discharging the significant capacitive loads on the AT Bus.

2. AT Bus Clock Generation

The Evergreen HV generates the AT Bus Clock by dividing down from the CLK2IN to an approximate 8 MHZ frequency. This has the distinct advantage of keeping the AT Bus Clock synchronous to the CPU clock, which removes the need for a second oscillator and simplifies the AT clock synchronization process. The appropriate divisor for the At Bus Clock depends on the speed of the CPU. The following table indicates the divisors supported and which apply at each CPU clock frequency to achieve an approximate 8MHZ Bus speed. The appropriate divisor must be selected by a configuration register option.

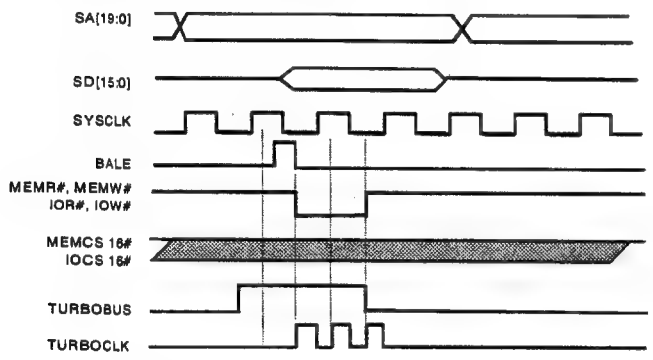
CPU Clock	CLK2IN	Divide CLK2IN by
16MHZ	32MHZ	4
20MHZ	40MHZ	5
25MHZ	50MHZ	6/7
33MHZ	66MHZ	8/9



At Bus 8-bit Access Timing

5-7. TurboBus

Many devices on the AT Bus are capable of operating at higher than the standard 8MHZ Bus speed. This generally presents a compatibility problem, with other devices on the Bus that cannot run any faster than 8MHZ. The PT86C368 provides a TurboBus option which provides a "best of both worlds" solution. This option allows selected devices to operate at higher speeds without compromising compatibility with slower devices. All devices are connected to the common AT Bus but the frequency of each AT Bus operation is determined by a programmable address decode to be either a standard frequency operation or a TurboBus operation. In addition, the PT86C368 provides a TURBOBUS control output which may be used to shield slower devices from being confused by the TurboBus cycles. Any Turbo devices should be connected directly to the PT86C368 command strobe outputs, while devices requiring the standard AT Bus speed should be connected to the output of the tri-stateable transceiver between the PT86C368 and the AT Bus. The output enable of this transceiver should be connected to the TURBOBUS control pin. The TURBOBUS signal will be driven high on any TurboBus cycle thereby disconnecting the command strobes of slower devices during high speed cycles. Aside from the reference speed of the bus cycle most bus mechanisms operate in the same manner as the standard 8MHZ AT Bus. Like the standard AT Bus speed, the TurboBus speed is also selected as a division of the CLK2IN frequency. The range of divisors supported is from 3 to 9.



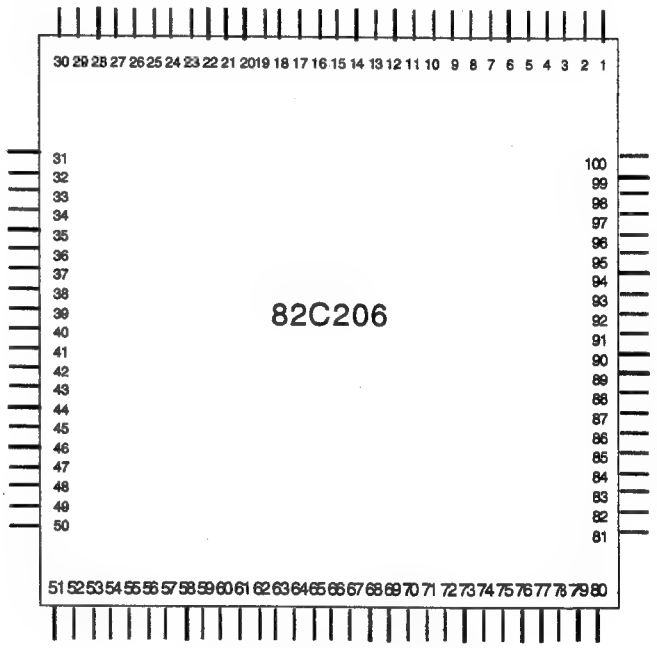
TURBOCLKIS AN INTERNAL CLOCK

TurboBus I -- 16 Bit Memory Cycle or
TurboBus II -- 8 or 16 Bit, Memory or I/O Cycles

6. 82C206 Integrated Peripheral Controller

6-1. General Description

The 82C206 Integrated Peripheral Controller includes two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, one MC146818 compatible real time clock, an additional 64 bytes CMOS RAM, one 74LS612 memory mapper, and some top level decoder/configuration logic circuits. It is a single chip integration of all main peripheral parts attached to the X bus of PC/AT architecture.
While providing full compatibility with PC/AT architecture, the 82C206 also offers some enhanced features and improved speed performance. These include an additional 64 bytes of user definable CMOS RAM in real time clock and drastically reduced recovery time for the 8237, 8259 and 8254. Programmable wait state option is provided for the DMA cycles and CPU I/O cycles accessing this chip. This chip also provides programmable 8 or 4 MHz DMA clock selection. The 82C206 is implemented using advanced 1.5u CMOS design technology and is packaged in an 100 Pin QFP.



Local DRAM Refresh in CPU Mode

6-2. Pin Description

Pin#	Designation	I/O	Description
15	SYSCLK	I	CLOCK INPUT is used to generate the timing signals for DMA operation. This pin can be driven to 10 MHz frequency. The internal clock used for DMA operation is either SYSCLK or SYSCLK/2 which is a
75	OSCI	I	OSCILLATOR INPUT is used to generate the time base for the time function of real time clock. External square waves of 32.768 KHz may be connected to this pin.
10	RESET	I	RESET is an active high input which affects the following registers: DMA controller: Clears the command, status, request, temporary registers, byte pointer flip flop. Sets the mask register. Following reset, DMA controller is in the idle state. INTERRUPT controller: Clears the edge sense circuit, mask registers, all ICW4 functions. IRQ0 is assigned the highest priority. Slave address is set to 7. Special mask mode is disable and status read is set to IRR.
71	IOCHARDY	I/O	I/O CHANNNEL READY is a bidirectional pin. In the input mode, it is used to extend the memory read or write pulses for the DMA controller to access slow memories or I/O devices. It must satisfy setup and hold times with respect to the DMA internal clock in order to work reliably. A low on IOCHRDY causes the internal DMA ready signal to go low asynchronously. When IOCHRDY goes high, one DMA clock cycle will elapse before internal DMA ready signal goes high. In the output mode, it is an open drain output and provides an active low output whenever a UM82C206 internal register is accessed. It will remain low for a pre-programmed unmber of DMA internal clock cycles (as controlled by bits 7 and 6 of UM82C206 configuration register) and then goes high. In this way, IOCHRDY can insert wait states (as counted by DMA internal clock cycles) when CPU accesses the UM82C206 internal registers. This pin must be pulled up by an external resistor. In a PC/At architecture base design this pin should be wire-ORed to the PC/AT's IOCHRDY signal.

Pin#	Designation		I/O	Description
24-31	18-25	XD7-XD0	I/O	X DATA BUS are 3-state bidirectional pins which are connected to the XD bus in PC/AT architecture design. During CPU I/O write cycles, these are input pins to let CPU program the contents of UM82C206 internal registers. During DMA cycles, the most significant 8 bits of the address are output onto these pins to be strobed into an external latch by ADSTB8 or ADSTB16. During DMA memory-to-memory transfers, data from the memory comes into the DMA controller via these pins and stores in the internal temporary register during read from the memory partial cycle. In the write to memory partial cycle, the data stored in the temporary register will output via these pins again and write into the new memory location. During the interrupt acknowledge cycle, the interrupt controllers outputthe interrupt vector byte via these pins. These pins are also used as the multiplexed address/data bus for the real time clock and the CMOS RAM accesses.
35-43 34	31-39 41	XA8-XA0 AX9	I/O I	ADDRESS BUS are connected to the XA bus in PC/AT architecture design. XA8-XA0 pins are bidirectional pins. XA9 is an input only pin. During CPU I/O accessesto the UM82C206, XA9-XA0 areused to address configuration register and the internal registers of 8237, 8259, 8254, MC146818, CMOS RAM, 74LS612. During a CPU cycle, XA3-XA0 pins are used by the CPUto address the registers of the DMA controller corresponding to DMA channels 0-3. XA4-XA1 pins are used by the CPUto address the registers of the DMA controller corresponding to DMA channels 5-7. During a DMA cycle, XA7-XA0 pins are outputs and carry address information for DMA channels 0-3. XA8-XA1 pins are outputs and carry address information for DMA channels 5-7.
54	54	$\overline{\text{XIOR}}$	I/O	X I/O READ is a bidirectional active low 3-state pin. In non DMA or non interrupt cycle, it is an input control signal used by the CPU to read the UM82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA controller to access data from a peripheral druing a DMA write memory transfer.

Pin#	Designation		I/O	Description
52	50	$\overline{XIOW}$	I/O	X I/O WRITE is a bidirectional active low 3 state pin. In a non DMA or non interrupt cycle, it is an input control signal used by the CPU to write the UM82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA controller to write data to a peripheral during a DMA read memory transfer.
61	61	$\overline{DMAMER}$	O	DMA MEMORY READ is an active low 3-state output pin used to access data from the selected memory location during DMA read memory or memory-to-memory transfer.
62	62	$\overline{DMAMEMW}$	O	DMA MEMORY WRITE is an active low 3-state outputpin used to write data to the selected memory location during DMA write memory or memory-to-memory transfer.
73	76	HLDA1	I	HOLD ACKNOWLEDGE 1 is an active high signal from the UM82C211C to indicate that the CPU has relinquished control of the system busses.
69	72	HRQ	O	HOLD REQUEST is an active high output to the UM82C211 to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the DMA controller issues HRQ to the UM82C211C. After CPU releases the system bus, the UM82C211C then issues a HLDA1 back to the UM82C206 if DMA has been permitted to control the system bus.
44-47	42-45	DREQ0-DREQ3 DREQ7	I	DMA REQUEST is an asynchronous DMA channel request input for each DMA channel. In fixed priority, DREQ0 has the highest priority and DREQ7. has the lowest priority. A Periphal device will activate a DREQ line if it needs a DMA service. DACK will acknowledge the recognition of DREQ request. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the DMA clock is stopped. Unused DREQ inputs should be kept inactive and the corresponding mask bit should be set to avoid an undesired DMA function. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ0-DREQ3 support 8-bit transfers between 8-bit I/O device and 8 or 16-bit transfers between 16-bit I/O device and 16-bit system memory. DERQ4 is not externally available and is used to cascade DREQ0-DREQ3.

Pin#	Designation		I/O	Description
67	70	TC	O	TERMINAL COUNT is an active high signal. It indicates the completion of DMA services. A pulse is generated by the DMA controller when terminal count for any channel is reached except for channel 0 in memory-to-memory transfer mode. Druing memory-to-memory transfer terminal count will be generated when the terminal count for channel 1 occurs. When a TC pulse occurs, the DMA controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status register will be set for the currently active channel unless the channel is programmed for auto-initialization. In that case, the mask bit remains clear.
48-51 57-55	46-49 57-55	DACK0- DACK3- DACK5- DACK7	O	DMA ACKNOWLEDGE is used to notify the individual peripherals when one has been granted a DMA cycle. Because these signals are used internally for cascading the DMA channels and for DMA page register selection, they must be programmed to active low and cannot be changed. Reset initializes them to active low.
66	69	ADSTB8	O	ADDRESS STROBE 8 is an active high output. It is used to latch the upper address byte XA8-XA15 for 8-bit peripheral devices. During DMA block transfers, ADSTB8 will only be issued when the upper address byte must be updated, thus speeding transfer through elimination of S1 states of DMA cycles. ADSTB8 is active for DMA channels 0-3.
65	65	ADSTB16	O	ADDRESS STROBE 16 is an active high output. It is used to latch the upper address byte XA9-XA16 for 16-bit peripheral devices. During DMA block transfers, ADSTB16 will only be issued when the upper address byte must be updated, thus speeding transfer through elimination of S1 states of DMA cycles. ADSTB16 is active for DMA channels 5-7.
63	63	AEN8	O	ADDRESS ENABLE 8 is an active low output. It is used to enable the latch of the upper address byte XA8-XA15 for 8-bit peripheral devices. It is inactive when external bus master controls the system
64	64	AEN16	O	ADDRESS ENABLE 16 is an active low output. It is used to enable the latch of the upper address byte XA9-XA16 for 16-bit peripheral devices. It is inactive when external bus master controls the system

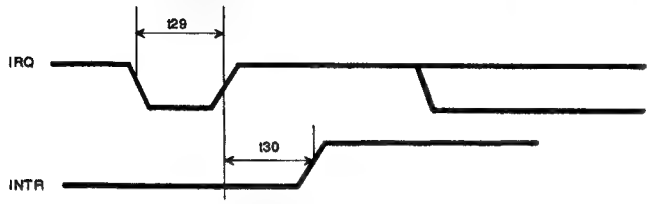
Pin#	Designation		I/O	Description
33	30	ACK (MSE)	I	MODULE SELECT ENABLE is a two purpose input. When high, it enables the chip select function on one of the modules of UM82C206 for the CPU programming functions. When low, the UM82C206 is essentially disconnected from the system bus and is capable of performing an active DMA or an interrupt cycle. In a PC/AT architecture design, it is tied to ACK signal of main board.
5-10 11 13	95-100 1 5	A23-A16 A17 XA16	O	A23-A17 and XA16 are 3-state output pins. A23-A17 are the upper 7 bits of the DMA page register. XA16 is the least significant bit of the DMA page register and is used for DMA transfers for 8-bit peripheral devices only. XA16 is not used for 16-bit DMA transfers as XA16-XA9 being provided by demultiplexing the data bus.
76-82 83 84 1-3 4	79-85 86 87 91-93 94	IRQ15-IRQ9 IRQ7 IRQ6 IRQ5-IRQ3 IRQ1	I	INTERRUPT RREQUESTS are asynchronous inputs. When 8259 is operating in edge triggered mode, an interrupt request is executed by raising an IRQ input low to high and holding it high until it is acknowledged by CPU. When 8259 is operating in level triggered mode, an interrupt request is executed by raising an IRQ input high and holding it high until it is acknowledged by CPU.
16	8	$\overline{\text{INTA}}$	I	INTERRUPT ACKNOWLEDGE is an active low input. It is used to enable the interrupt controllers to output the vector data on to the data bus by an interrupt acknowledge sequence from the CPU.
70	73	INTR	O	INTERRUPT REQUEST is an active high output pin. It is connected to the CPU's interrupt pin and is used to interrupt the CPU when an interrupt request occurs.
23	17	TMRCLK	I	TIMER CLOCK is an input clock for 8254 counter 0, counter 1 and counter 2. In PC/AT architecture design, it is approximately 1.19 MHz.
22	16	GATE2	I	GATE 2 is a gate input for 8254 counter 2. In PC/AT architecture design, the counter 2 is used for tone generation for speaker. It is driven by bit 0 of I/O port 61 h.
20	14	OUT1	O	OUT 1 is an output of 8254 counter 1. In PC/AT architecture design, the counter 1 is programmed as a rate generator to produce a 15 usec period signal for DRAM refresh.
19	13	OUT2	O	OUT 2 is an output of 8254 counter 2. In PC/AT architecture design, counter 2 is used for tone generation for speaker.

Pin#	Designation		I/O	Description
71	74	AS	I	ADDRESS STROBE is an active high input. It is pulsed by UM82C211C when CPU accesses the real time clock or CMOS RAM of the UM82C206. The falling edge of this pulse latches the address from the XD bus.
15	7	$\overline{\text{PSRSTB}}$	I	POWER SUPPLY STROBE is an active low input. It is used to establish the condition of the control registers of real time clock when power is applied to the device. In PC/AT architecture design, it should be tied to the battery back-up circuit. When PSRSTB and TEST are both low, the following occurs: (a) Periodic Interrupt Enable (PIE) bit is cleared to zero. (a) Periodic Interrupt Enable (PIE) bit is cleared to zero. (b) Alarm Interrupt Enable (AIE) bit is cleared to zero. (c) Update ended Interrupt Enable (UIE) bit is cleared to zero. (d) Update ended Interrupt Flag (UF) bit is cleared to zero. (e) Interrupt Request status Flag (IRQF) is cleared to zero. (f) Periodic Interrupt Flag (PF) bit is cleared to zero. (g) The part is not accessible. (h) Alarm Interrupt Flag (AF) bit is cleared to zero. (i) Square Wave output enable bit is cleared to zero.
14	6	PWRG		POWER GOOD is an active high input and is connected to the power good of the power supply in PC/AT architecture design. It must be high for bus cycles in which the CPU accesses the real time clock. When it is low, all address, data, data strobe and R/W pins are disconnected from the processor.
17	9	TEST	I	TEST is an active high input to enable the chip testing for production. It should be tied low for normal operation.
32,75	26,78	VCC		POWER SUPPLY
12,53 7 4	3,77 52	VSS		GROUND

6-3. Interrupt Controller

Description

There are two programmable interrupt controllers for the 82C206. They are fully compatible with Intel's 8259 controller, providing up to 15 interrupts sources (14 external and 1 internal). The internal line connects to the 8254 Counter 0 output. These interrupt controllers prioritize interrupt requests to the CPU.



Interrupt Timing

(1) Interrupt Controller Channel Assignment

IRQ 0 - Timer Channel 0
IRQ 1 - Keyboard (Output Buffer Full)
IRQ 2 - Interrupt from Controller 2
IRQ 3 - Serial Port (Secondary)
IRQ 4 - Serial Port (Primary)
IRQ 5 - Parallel Port 2
IRQ 6 - FDD Controller
IRQ 7 - Parallel Port 1
IRQ 8 - Real Time Clock Interrupt
IRQ 9 - Software Redirected to INTOAH (IRQ2)
IRQ 10 - Reserved
IRQ 11 - Reserved
IRQ 12 - Reserved
IRQ 13 - Co-processor
IRQ 14 - HDD Controller
IRQ 15 - Reserved

6-4. DMA

Description

The 82C206 has two DMA controllers, compatible with the Intel 8237, which provide a total of seven DMA channels.
Combined with the Memory Mapper, each DMA channel has a 24-bit address output to access data throughout the 16MB system address space. Channel 0 through channel 3 support 8-bit peripherals, transferring data to or from an 8-bit memory. Each channel can transfer data in 64kB pages. Channel 4 is used for cascading and is not available externally. Channel 5 through channel 7 support 16-bit I/O adapters, transferring data a word at a time. These channels can transfer in 128kB pages.

DMA Channel No.	Function
0	Spare
1	SLDC
2	Diskette
3	Spare
4	Spare
5	Spare
6	Spare
7	Spare

* Synchronous Data Link Control Communication

6-5. Memory Mapper

The 82C206 has a built-in equivalent logic to the 74LS612, generating the upper address bits during a DMA cycle.

Source Memory Mapper 8237
(for DMA Channels 0-3)
Address A23 <--------- >A16 A15 <--------- >A0
(For DMA Channels 5-7)
Address A23 <--------- >A17 A16 <--------- >A1

6-6. Timer/Counter

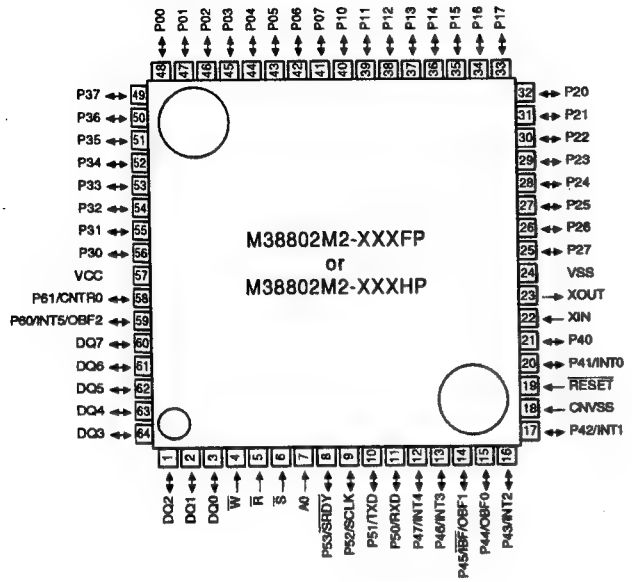
The 82C206 provides three internal counters which are compatible with the 8254. The clock input for each counter is tied to a clock of 1.19MHz, which is derived by dividing the 14.318MHz crystal input by 12. The output of Counter 0 is connected to the IRQ0 input of interrupt controller 1. Counter 1 initiates a refresh cycle and Counter 2 generates sound waveforms for the speaker.

6-7. I/O Address Map

Hexadecimal Range	Devices	Usag
000-01F	DMA controller 1	System
020-03F	Interrupt controller 1	System
040-05F	Timer	System
060-06F	Keyboard I/O	System
070-07F	Real time clock, NMI mask	System
080-09F	DMA page register	System
0A0-0BF	Interrupt controller 2	System
0C0-0DF	DMA controller 2	System
0F0	Clear math coprocessor busy	System
0F1	Reset math coprocessor	System
0F8-0FF	Math coprocessor	System
1F0-1F8	Fixed disk	I/O
200-207	Game	I/O
278-27F	Parallel printer port 2	I/O
2F8-2FF	Serial port 2	I/O
300-31F	Prototype card	I/O
360-36F	Reserved	I/O
378-37F	Parallel printer port 1	I/O
380-38F	SDLC, Bi-synchronous 2	I/O
3A0-3AF	Bi-synchronous 1	I/O
3B0-3BF	Mono display printer adapter	I/O
3C0-3CF	Reserved	I/O
3D0-3DF	Color/graphic monitor adapter	I/O
3F0-3F7	Floppy diskette controller	I/O
3F8-3FF	Serial port 1	I/O

7. M38802M2 Keyboard Encoder

Pin configuration (Top view)

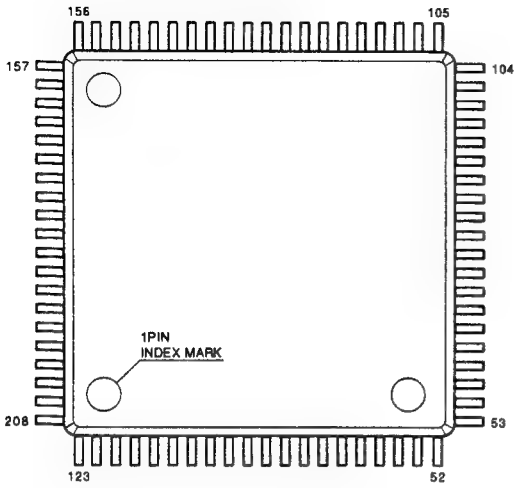


Pin description

Pin	Name	Function	Alternate Function
C_{CC}, V_{SS}	Power supply	Power supply inputs 2.7 to 5.5V to V_{CC} and 0V to V_{SS}.	
CNV_{SS}	CNV_{SS}	This pin controls the operation mode of the chip. Normally connected to V_{SS}.	
$\overline{RESET}$	Reset input	To reset the microcomputer, this pin should be kept at an "L" level for more than 2μs under normal operating conditions.	
X_{IN}	Clock input	Input and output signals for the internal clock generation circuit. Connect a ceramic resonator or quarts crystal between the X_{IN} and X_{OUT} pins to set the oscillation frequency. If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0$–$P0_7$	I/O port P0	An 8-bit I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. The output structure of this port is CMOS 3-state, and the input levels are CMOS compatible.	
$P1_0$–$P1_7$	I/O port P1		
$P2_0$–$P2_7$	I/O port P2	An 8-bit I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. The output structure of this port is CMOS 3-stale, and the input levels are CMOS compatible. $P2_4$–$P2_7$ (4 bits) are enabled to output large current for LED drive.	
$P3_0$–$P3_7$	I/O port P3	An 8-bit I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. The output structure of this port is CMOS 3-state, and the input levels are CMOS compatible. PUll-up control is enabled.	Key-on wakeup input pins Analog input pins
$P4_0$	I/O port P4	An 8-bit I/O port with the same function as port P0. Switching of CMOS/TTL input level is enabled. The output structure of this port is enabled to switch CMOS 3-state/N-channel open drain. In spite of setting input or output port, input of each pin is enabled.	
$P4_1/INT_0$, $P4_2/INT_1$, $P4_3/INT_2$			Interrupt input pins
$P4_4/OBF_0$, $P4_5/\overline{IBF}$/ OBF_1			Data bus buffer function pins
$P4_5/INT_3$, $P4_7/INT_4$			Interrupt input pins
$P5_0/R_XD$, $P5_1/T_XD$, $P5_2/S_{CLK}$, $P5_3/\overline{SRDY}$	I/O port P5	A 4-bit I/O port with the same function as port P0. The output structure of this port is CMOS 3-state, and the input levels are CMOS compatible.	Serial I/O function pins
$P6_0/INT_5/OBF_2$	I/O port P6	A 2-bit I/O port with the same function as port P0. The output structure of this port is CMOS 3-state, and the input levels are CMOS compatible.	Interrupt input pin/ Data bus buffer function pin
$P6_1/CNTR_0$			Timer X function pin
A0, $\overline{S}$, E/R, R/$\overline{W}$/$\overline{W}$	Input port	Control bus for host CPU. Switching of CMOS/TTL input level is enabled.	
DQ_0–DQ_7	I/O port	An 8-bit data bus for host CPU. Switching of CMOS/TTL. Input level is enabled.	

8. VADEM468 PCMCIA Controller

(1) Pin Diagram



Signal Description

Pin #	Signal Names	Type	Characteristics	# Pins
204	AEN	I	TTL Compatible	1
205	BALE	I	TTL Compatible	1
54, 125	BVD1 (*STSCHG/*RI)	I	CMOS Schmitt Trigger	2
52, 123	BVD2 (*SPKR)	I	CMOS Schmitt Trigger	2
15, 19, 21, 23-26, 28, 29, 31, 33-41, 43, 44, 46, 48, 50, 51, 53, 86, 90, 92, 94-99, 102, 104-107, 109-115, 117, 119, 121, 122, 124	CA[25:0]	O	4mA Tri-State	52
63, 3, 134, 74	*CD[2:1]	I	CMOS Schmitt Trigger	4
89, 83, 18, 11	*CE[2:1]	O	4mA Tri-State	4
187	CLK	I	TTL Compatible	1
2, 4-10, 12, 13, 55-58, 60, 62, 73, 76-82, 84, 85, 126-130, 133	D[15:0]	I/O	I = TTL Compatible O = 4mA Output	32
14, 27, 42, 75, 101, 131, 135, 154, 169, 188	GND			10
67, 68	GPIO	I/O	I = CMOS Schmitt Trigger O = 4mA Tri-State	2
49, 120	*INPACK	I	TTL Compatible	2
152	*INTR	I/O	I = TTL Compatible O = 4mA Tri-State	1
150	IOCHRDY	O	16 mA Tri-State	1
148	*IOCS16	O	16 mA 5V Open Drain	1
20, 91	*IORD	O	4mA Tri-State	2
22, 93	*IOWR	O	4mA Tri-State	2
136-140, 146-142	IRQs	O	4mA Tri-State	10
181-175	LA[23:17]	I	TTL Compatible	7
149	*MEMCS16	O	16 mA 5V Open Drain	1
174	*MEMR	I	TTL Compatible	1
173	*MEMW	I	TTL Compatible	1
16, 87	*OE	O	4mA Tri-State	2
208	PWRGOOD	I	Schmitt Trigger	1
32, 103	RDY/*BSY (*IREQ)	I	CMOS Schmitt Trigger	2
1, 72	*REG	O	4mA Tri-State	2
45, 116	RESET	O	4mA Tri-State	2
189	RESETDRV	I	Schmitt Trigger with pull-down	1
151	*RIO/LED	I/O	I = TTL Compatible O = 4mA Tri-State	1
203-192, 190, 186-183	SA[16:0]	I	TTL Compatible	17
182	*SBHE	I	TTL Compatible	1
206	*SIOR	I	TTL Compatible	1
207	*SIOW	I	TTL Compatible	1
155-162, 172-170, 168, 167, 165-163	SD[15:0]	I/O	I = TTL Compatible O = 8mA Tri-State	16
153	*SPKROUT	I/O	I = TTL Compatible O = 4mA Tri-State	1
17, 59, 88, 108, 141, 166, 191	VCC			7
66, 69	*VCCEN	O	4mA Output	2
65, 70	VPP1EN1	O	4mA Output	2
64, 71	VPP2EN1	O	4mA Output	2
47, 118	*WAIT	I	TTL Compatible	2
30, 100	*WE/*PRGM	O	4mA Tri-State	2
61, 132	WP (*IOIS16)	I	TTL Compatible	2
147	*ZWS	O	16mA 5V Open Drain	1

Pin Description

Symbol	Type	Pin No.	Description
RESET	O	45,116	Provides a hard reset to a PC Card and clears the Card Configuration Option Register, thus placing card in an unconfigured (memory interface) state.
RESETDRV	I	189	Active high indicates a main system reset.
*RIO/LED	I/O	151	Ring Indicate Output. Pass through of Ring Indicate output from I/O PC Card. VG-468 can also be configured to activate *RIO on card detect changes. *RIO will be functional in *CS controlled power down. When disk drive LED enable is set this signal becomes a driver for disk drive LED. Also, a resistor strapping input during RESETDRV to determine the functions of pin B_CA[11:4].
SA[16:0]	I	203-192, 190, 186-183	System Address bus used to address memory and I/O devices on the ISA bus. These signals are latched and are valid throughout the bus cycle.
*SBHE	I	182	System Byte High Enable. When asserted, this active low signal indicates that a data transfer is occurring on the upper byte of the system data bus.
SD[7:0]	I/O	155-162, 172-170, 168, 167, 165-163	System Data Bus.
*SIOR	I	206	This active low I/O read signal instructs the VG-468 to drive data onto the data bus.
*SIOW	I	207	This active low I/O write signal instructs the VG-468 to latch the data on the data bus.
*SPKROUT	I/O	153	Digital audio signal which provides a single amplitude (digital) audio waveform to drive the system's speaker. Passes through "SPKR from an I/O PC Card. This signal must be held high when no audio signal is present. Also, a resistor strapping input during RESETDRV to determine the mapping of socket A and socket B to one of four groups.
*CD[2:1]	I	63, 3, 134, 74	Detects proper card insertion. The signals are connected to ground internally on the PC Card and will be forced low whenever a card is placed in a host socket. Status is available to software through the Interface Status Register.
*CE[2:1]	O	89, 83, 18, 11	Active low card enable signals. *CE1 is used to enable even bytes, *CE2 for odd bytes. A multiplexing scheme based on A0, *CE1, *CE2 allows 8-bit hosts to access all data on Card Data[7:0] if desired.
CLK	I	187	System clock.
D[15:0]	I/O	2, 4-10, 12, 13, 55-58, 60, 62, 73, 76-82, 84, 85, 126-130, 133	Card data.
GPIO	I/O	67, 68	General purpose input/output. May be used for one of several purposes. • An active low input indicates that Vpp power line has reached the user specified range. • An input indication a card eject or card insertion pending. • An input source for generating a card status change interrupt. • Programmable chip select output.
*INPACK	I	49, 120	Input Acknowledge. Asserted by some PC Cards during I/O read cycles. This signal is used by the VG-468 to control the enable of its input data buffer between the card and CPU.
*INTR	I/O	152	Interrupt Request output: Active low output requesting a nonmaskable interrupt to the CPU. Also, a resistor strapping input during RESETDRV to determine the mapping of socket A and socket B to one of four groups.

Symbol	Type	Pin No.	Description
IOCHRDY	O	150	I/O Channel Ready. This active high signal indicates that the current I/O bus cycle has completed. When a PC Card needs to extend a Read or Write cycle, the VG-468 pulls IOCHRDY low. IOCHRDY can be deasserted by either *WAIT, or by programming to add wait states for 16-bit memory and I/O cycles. If *WAIT is used in 16-bit mode, the wait state generator has to be set to 1 wait state.
*IOCS16	O	148	This active low I/O 16-bit chip select signal indicates to the host system the current I/O cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.
*IORD	O	20, 91	I/O Read signal is driven active to read data from the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
*IOWR	O	22, 93	I/O Write signal is driven active to write data to the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
IRQs	O	136-140, 146-142	IRQ[15, 14, 12:9, 7, 5:3].
LA[23:17]	I	181-175	Local Address bus used to address memory devices on the ISA-bus. Together with the system address signals, they address up to 16MB on the ISA bus.
*MEMCS16	O	149	This active low 16-bit memory chip select signal indicates to the host system that the current memory cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.
*MEMR	I	174	Active low signal indicates a memory read cycle.
*MEMW	I	173	Active low signal indicates a memory write cycle.
*OE	O	16, 87	Active low signal used to gate memory reads from memory cards.

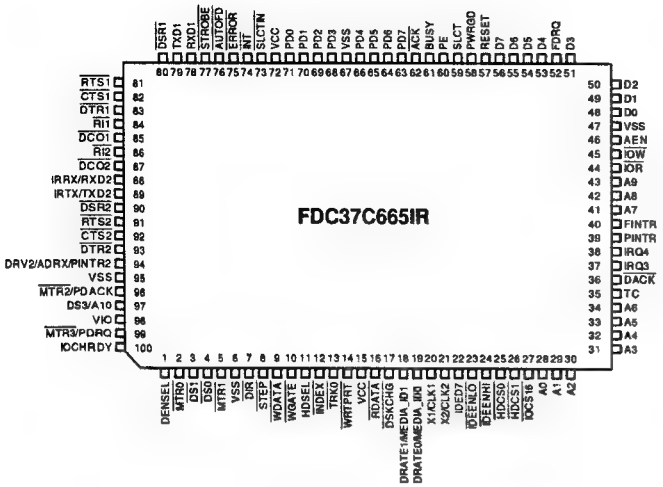
Symbol	Type	Pin No.	Description
PWRGOOD	I	208	Power Good is an active high signal which indicates that power to the system is stable. Combined with RESETDRV, it will indicate to VG-365 whether a cold reset, or a resume reset has occurred, to decide whether to reset the slot configuration registers. System implementations without a "POWER GOOD" as resume indication should tie this signal low.
RDY/*BSY (*IREQ)	I	32, 103	Memory PC Cards drive Ready / *Busy low to indicate that the memory card circuits are busy processing a previous write command. It is set high when they are ready to accept a new data transfer command. For I/O PC Cards, this pin is used as an interrupt request and driven low to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested.
*REG	O	1, 72	Select attribute memory. This signal is set inactive (high) for all accesses to common memory of a PC Card. When it is active, access is limited to Attribute Memory when *WE or *OE are active, and to I/O ports when *IORD or *IOWR are active. I/O PC Cards will not respond to *IORD or *IOWR when the *REG signal is inactive. During DMA operations the *REG signal is inactive.
AEN	I	204	System Address enable. High during DMA cycles, low otherwise.
BALE	I	205	Bus Address Latch Enable. An active high input used to latch LA[23:17] at the beginning of a bus cycle.

Symbol	Type	Pin No.	Description
BVD1 (*STSCHG/*RI)	I	54, 125	If BVD1 is negated by a memory PC Card with a battery, it indicates that the battery is no longer serviceable and data is lost. For I/O PC Cards, this signal is held high when either or both the Signal on Change bit and Changed bit in the Card Status Register on the PC Card are set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. Or this pin is connected to Ring Indicate, which is qualified by Ring Indicate Enable to be passed on to the *RIO pin.
BVD2 (*SPKR)	I	54, 123	BVD1 and BVD2 are generated by memory PC Cards with onboard batteries. These signals indicate the health of the battery. Both are asserted high when the battery is in good condition. When BVD2 is negated while BVD1 is still asserted, the battery should be replaced, although data integrity on the memory PC Card is still assured. When the I/O interface is selected, BVD2 may be used to provide a single amplitude Digital Audio waveform intended to be passed through to the system's speaker without signal conditioning.
CA[25:0]	O	15, 19, 21, 23-26, 28, 31, 33-41, 43, 44, 46, 48, 50, 51, 53, 86, 90, 92, 94-99, 102, 104-107, 109-115, 117, 119, 121, 122, 124	Card Address.
*VCCEN	O	66, 69	Power Control signal for card Vcc.
VPP1EN1	O	65, 70	Power Control signal for card Vpp1.
VPP2EN1	O	64, 71	Power Control signal for card Vpp2.
*WAIT	I	47, 118	This signal is driven by the PC Card to delay completion of the memory or I/O cycle in progress.

Symbol	Type	Pin No.	Description
*WE/*PRGM	O	30, 100	The host uses *WE for gating memory write data, and for memory PC Cards that employ programmable memory.
WP (*IOIS16)	I	61, 132	Reflects the status of the Write Protect switch on some memory PC Cards. If the memory PC Card has no write protect switch, the card will connect this line to ground (the card can always be written) or to Vcc (permanently write protected). When the I/O interface is selected, this pin is used for the "I/O is 16-bit Port" function: asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port which is addressed is capable of 16-bit access. If this signal is not asserted during a 16-bit I/O access, the system will generate 8-bit references to the even and odd byte of the 16-bit port being accessed. If 8-bit window size is selected, *IOIS16 is ignored.
*ZWS	O	147	Zero Wait State. An active low output indicates that the PC Card wishes to terminate the present bus cycle without inserting additional wait states. This cycle will not be driven during a 16-bit I/O access.

9. FDC 3TC665 Super Multi-I/O Chip

Pin configuration



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
		HOST PROCESSOR INTERFACE		
48 ~ 51 53 ~ 56	Data Bus 0 ~ 7	D0 ~ D7	I/O12	The data bus connection used by the host microprocessor to transmit data to and from the FDC37C665IR. These pins are in a high-impedance state when not in the output mode.
44	I/O Read	$\overline{IOR}$	I	This active low signal is issued by the host microprocessor to indicate a read operation.
45	I/O Write	$\overline{IOW}$	I	This active low signal is issued by the host microprocessor to indicate a write operation.
46	Address Enable	AEN	I	Active high Address Enable indicates DMA operations on the host data bus. Used internally to qualify appropriate address decodes.
28 ~ 34 41 ~ 43	I/O Address	A0 ~ A9	I	These host address bits determine the I/O address to be accessed during $\overline{IOR}$ and $\overline{IOW}$ cycles. These bits are latched internally by the leading edge of $\overline{IOR}$ and $\overline{IOW}$.
52	FDC DMA Request	FDRQ	O12	This active high output is the DMA request for byte transfers of data to the host. This signal is cleared on the last byte of the data transfer by the $\overline{DACK}$ signal going low (or by $\overline{IOR}$ going low if $\overline{DACK}$ was already low as in demand mode).
36	DMA Acknowledge	$\overline{DACK}$	I	An active low input acknowledging the request for a DMA transfer of data. This input enables the DMA read or write internally.
35	Terminal Count	TC	I	This signal indicates to the FDC37C665IR that data transfer is complete. TC is only accepted when $\overline{DACK}$ or $\overline{PDACK}$ is low. In AT and PS/2 model 30 modes, TC is active high and in PS/2 mode, TC is active low.
38	Serial Port Interrupt Request	IRQ4	O12	IRQ4 is the interrupt from the Primary Serial Port (PSP) or Secondary Serial Port (SSP) when the PSP or SSP have their address programmed as COM1 or COM3 (as defined in the Configuration Registers). The appropriate interrupt from the Serial Port is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset.
	Primary Serial Port Interrupt	PSPIRQ	O12	FDC37C666IR (Adapter application): PSPIRQ is a source of PSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers.
37	Serial Port Interrupt Request	IRQ3	O12	IRQ3 is the interrupt from the Primary Serial Port (PSP) or secondary Serial Port (SSP) when the PSP or SSP have their address programmed as COM2 or COM4 (as defined in the Configuration Registers). The appropriate interrupt from the Serial Port is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset.
	Secondary Serial Port Interrupt	SSPIRQ	O12	FDC37C666IR (Adapter application): SSPIRQ is a source of SSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers.
40	Floppy Controller Interrupt Request	FINTR	O12	This interrupt from the Floppy Disk Controller is enabled/disabled via bit 3 of the Digital Output Register (DOR).
39	Parallel Port Interrupt Request 1	PINTR1	O12	This interrupt from the Parallel Port is enabled/disabled via bit 4 of the Parallel Port Control Register. Refer to configuration registers CR1 and CR3 for more information.
			OD12	If EPP or ECP Mode is enabled, this output is pulsed low, then released to allow sharing of interrupts.

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
		HOST PROCESSOR INTERFACE		
57	Reset	RST	IS	This active high signal resets the FDC37C665IR and must be valid for 500 ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset. In the FDC37C666IR, the falling edge of reset latches the jumper configuration. The jumper select lines must be valid.
		FLOPPY DISK INTERFACE		
16	Read Disk Data	RDATA	IS	Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data.
10	Write Gate	WGATE	OD20	This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
9	Write Data	WDATA	OD20	This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
11	Head Select	HDSEL	OD20	This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.
7	Direction Control	DIR	OD20	This high current low active output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.
8	Step Pulse	STEP	OD20	This active low high current driver issues a low pulse for each track-to-track movement of the head.
17	Disk Change	DSKCHG	IS	This input senses that the drive door is open or that the diskette has possible been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H.
4, 3	Drive Select 0, 1	DS0, 1	OD20	Active low open drain outputs select drives 0 ~ 1. Refer to Note 2.
97	Drive Select 3	DS3	OD20	In non-ECP mode: Active low open drain output selects drive 3. Refer to Note 2.
	I/O Address 10	A10	I	In ECP Mode, this pin is the A10 address input.
2, 5	Motor On 0, 1	MTR0, 1	OD20	These active low open drain outputs select motor drives 0 ~ 1. Refer to Note 1.
96	Motor On 2	MTR2	OD20	Motor On 2: Refer to Note 1.
		PDACK	I	In ECP Mode, MTR2 is the Parallel Port DMA Acknowledge input. Active Low.
99	Motor On 3	MTR3	OD20	Motor On 3: Refer to Note 1.
		PDRQ	O12	In ECP Mode, MTR3 is the Parallel Port DMA Request Output. Active High.
1	Density Select	DENSEL	OD20	Indicates whether a low (250/300 Kb/s) or high (500 Kb/s) data rate has been selected. This is determined by the IDENT bit in Configuration Register 3.
14	Write Protected	WRTPRT	IS	This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored.
13	Track 00	TR0	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.
12	Index	INDEX	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
19, 18	Data Rate 0, Data Rate 1	DRATE0, DRATE1	O4	These two outputs reflect bits 0 and 1 respectively of the Data Rate Register. At power on, these two outputs are in a high impedance state.
	Media ID0, Media ID1	MEDIA_ID0 MEDIA_ID1	I	In Floppy Enhanced Mode 2 - These bits are the Media ID 0, 1 inputs. The value of these bits can be read as bits 6 and 7 of the Floppy Tape register.
		SERIAL PORT INTERFACE		
78 88	Receive Data	RXD1 RXD2/IRRX	I	Receiver serial data input or IR data input.
79	Transmit Data	TXD1	O2	Transmitter serial data output from Primary Serial Port.
		PCF0	I	FDC37C666IR (Adapter Mode): Parallel Port Configuration Control 0. During reset active this input is read and latched to define the address of the Parallel Port.

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
81	Request to Send	$\overline{RTS1}$	O2	Active low Request to Send output for Primary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the $\overline{RTS}$ signal to inactive mode (high). Forced inactive during loop mode operation.
	Parallel Port Configuration Control	PCF1	I	FDC37C666IR (Adapter Mode): Parallel Port Configuration Control 1. During reset active this input is read and latched to define the address of the Parallel Port.
		SERIAL PORT INTERFACE		
91	Request to Send	$\overline{RTS2}$	O2	Active low Request to Send output for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the $\overline{RTS}$ signal to inactive mode (high). Forced inactive during loop mode operation.
	Secondary Serial Port Configuration Control	S2CF0	I	FDC37C666IR (Adapter Mode): Secondary Serial Port Configuration Control 0. During reset active this input is read and latched to define the address of the Secondary Serial Port.
83	Data Terminal Ready	$\overline{DTR1}$	O2	Active low Data Terminal Ready output for primary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the $\overline{DTR}$ signal to inactive mode (high). Forced inactive during loop mode operation.
	IDE Configuration Control	IDECF	I	FDC37C666IR (Adapter Mode): IDE Configuration Control. During reset active this input is read and latched to enable/disable the IDE.
93	Data Terminal Ready	$\overline{DTR2}$	O2	Active low Data Terminal Ready output for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR), The hardware reset will reset the $\overline{DTR}$ signal to inactive mode (high). Forced inactive during loop mode operation.
	Secondary Serial Port Configuration Control 1	S2CF1	I	FDC37C666IR (Adapter Mode): Secondary Serial Port Configuration Control 1. During reset active this input is read and latched to define the address of the Secondary Serial Port.
89	Transmit Data 2	TXD2	O2	Transmitter Serial Data output from Secondary Serial Port.
		IRTX	O12	Transmitter Serial IR Data output from Secondary Serial Port.
	Floppy disk Configuration	FDCCF	I	FDC37C666IR (Adapter Mode): Floppy Disk Configuration. This input is read and latched during reset to enable/disable the Floppy Disk Controller.
82, 92	Clear to Send	$\overline{CTS1}$, $\overline{CTS2}$	I	Active low Clear to Send inputs for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of $\overline{CTS}$ signal by reading bit 4 of Modem Status Register (MSR). A $\overline{CTS}$ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{CTS}$ changes state. The $\overline{CTS}$ signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of $\overline{CTS}$.
80, 90	Data Set Ready	$\overline{DSR1}$, $\overline{DSR2}$	I	Active low Data Set Ready inputs for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of $\overline{DSR}$ signal by reading bit 5 of Modem Status Register (MSR). A $\overline{DSR}$ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{DSR}$ changes state. Note: Bit 5 of MSR is the complement of $\overline{DSR}$.
85, 87	Data Carrier Detect	$\overline{DCD1}$, $\overline{DCD2}$	I	Active low Data Carrier Detect inputs for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of $\overline{DCD}$ signal by reading bit 7 of Modem Status Register (MSR). A $\overline{DCD}$ signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{DCD}$ changes state. Note: Bit 7 of MSR is the complement of $\overline{DCD}$.
84, 86	Ring Indicator	$\overline{RI1}$, $\overline{RI2}$	I	Active low Ring Indicator input for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of $\overline{RI}$ signal by reading bit 6 of Modem Status Register (MSR). A $\overline{RI}$ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{RI}$ changes state. Note: Bit 6 of MSR is the complement of $\overline{RI}$.

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
			SERIAL PORT INTERFACE	
94	Drive 2	DRV2	I/O2	In PS/2 mode, this input indicates whether a second drive is connected; DRV2 should be low if a second drive is connected. This status is reflected in a read of Status Register A. (Only available in FDC37C665IR. This pin must not be driven in the FDC37C666IR.)
	$\overline{\text{ADRx}}$	$\overline{\text{ADRx}}$	O2	Optional I/O port address decode output. Refer to Configuration registers CR3, CR8 and CR9 for more information. Active low. (Available in FDC37C665IR and FDC37C666IR.) Defaults to tri-state after power-up. This pin has a 30ua internal pull-up.
	Parallel Port Interrupt Request 2	PINTR2	O12	This interrupt from the Parallel Port is enabled/disabled via bit 4 of the Parallel Port Control Register. Refer to configuration registers CR1 and CR3 for more information.
	Enhanced Parallel Port Enable	ECPEN	I	FDC37C666IR (Adapter Mode): Enhanced Parallel Port mode select. Refer to FDC37C666IR hardware configuration for more information. Read and latched during reset active.
			PARALLEL PORT INTERFACE	
73	$\overline{\text{Printer Select Input}}$	$\overline{\text{SLCTIN}}$	OD12	This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register.
			OP12	Refer to Parallel Port description for use of this pin in ECP and EPP mode.
74	$\overline{\text{Initiate Output}}$	$\overline{\text{INIT}}$	OD12	This output is bit 2 of the printer control register. This is used to initiate the printer when low.
			OP12	Refer to Parallel Port description for use of this pin in ECP and EPP mode.
76	$\overline{\text{Autofeed Output}}$	$\overline{\text{AUTOFD}}$	OD12	This output goes low to cause the printer to automatically feed one line after each line is printed. The $\overline{\text{AUTOFD}}$ output is the complement of bit 1 of the Printer Control Register.
			OP12	Refer to Parallel Port description for use of this pin in ECP and EPP mode.
77	$\overline{\text{Strobe Output}}$	$\overline{\text{STROBE}}$	OD12	An active low pulse on this output is used to strobe the printer data into the printer. The $\overline{\text{STROBE}}$ output is the complement of bit 0 of the Printer Control Register.
			OP12	Refer to Parallel Port description for use of this pin in ECP and EPP mode.
61	Busy	BUSY	I	This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
62	$\overline{\text{Acknowledge}}$	$\overline{\text{ACK}}$	I	A low active output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the $\overline{\text{ACK}}$ input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
60	Paper End	PE	I	Another status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
59	Printer Selected Status	SLCT	I	This high active output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
75	$\overline{\text{Error}}$	$\overline{\text{ERR}}$	I	A low on this input from the printer indicates that there is a error condition at the printer. Bit 3 of the Printer Status register reads the $\overline{\text{ERR}}$ input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
71 ~ 68 66 ~ 63	Port Data	PD0 ~ PD7	I/OP12	The bi-directional parallel data bus is used to transfer information between CPU and peripherals.
100	IOCHRDY	IOCHRDY	OD12P	In EPP mode, this pin is pulled low to extend the read/write command. This pin has an internal pull-up.
			IDE	
23	$\overline{\text{IDE Low Byte Enable}}$	$\overline{\text{IDEENLO}}$	O2	This active low signal is used in both the XT and AT mode. In the AT mode, this pin is active when the IDE is enabled and the I/O address is accessing 1F0H ~ 1F7H and 3F6H ~ 3F7H in primary address mode or 170H ~ 177H and 376H, 377H in secondary address mode. In the XT mode, this signal is active for accessing 320H-323H, 8 bit programmed I/O or DMA.
	Primary Serial Configuration 1	S1CF1	I	FDC37C666IR (Adapter Mode): Primary Serial configuration 1. Read and latched during reset active to select the address of the Secondary Serial Port.
24	$\overline{\text{IDE High Byte Enable}}$	$\overline{\text{IDEENHI}}$	O2	This signal is active low only in the AT mode, and when IO16CSB is also active. The I/O addresses for which this pin reacts are 1F0H ~ 1F7H in primary address mode or 170H ~ 177H in secondary address mode. This pin is not used in XT mode.
	Primary Serial Configuration 0	S1CF0	I	FDC37C666IR (Adapter Mode): Primary Serial Configuration 0. Read and latched during reset active to define the address of the Secondary Serial Port.

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
				IDE
25	Hard Disk Chip Select	HDCSO	O12	This is the Hard Disk Chip select corresponding to addresses 1F0H ~ 1F7H in primary address mode or 170H ~ 177H in secondary address mode in the AT mode and addresses 320H ~ 323H in the XT mode.
	IDE Address Control	IDEACF	I	FDC37C666IR(Adapter Mode): IDE Address Control. Refer to FDC37C666IR hardware configuration for more information. Read and latched during reset active.
26	Hard Disk Chip Select	HDCS1	O12	This is the Hard Disk Chip select corresponding to 3F6H, 3F7H for primary address mode or 376H, 377H for secondary address mode in the AT mode and addresses 3F6H, 3F7H in the XT mode.
	Floppy Disk Address Control	FACF	I	FDC37C666IR (Adapter Mode): Floppy Disk Address Control. Refer to FDC37C666IR hardware configuration for more information. Read and latched during reset active.
27	I/O 16 Bit Indicator	IOCS16	I	This input indicates, in AT mode only, when 16 bit transfers are to take place. This signal is generated by the hard disk interface. Logic "0" = 16 bit mode; logic "1" = 8 bit mode.
		HDACK	I	In the XT mode, this is the Hard Disk Controller DMA Acknowledge, low active.
22	IDE Data Bit 7	IDED7	I/O12	IDE data bit 7 in the AT mode. IDED7 transfers data at I/O addresses 1F0H ~ 1F7H (R/W), 3F6 (R/W), 3F7 (W). IDED7 should be connected to IDE data bit 7. The FDC37C665IR functions as a buffer transferring data bit 7 between the IDE device and the host, during I/O read of 3F7H, IDED7 is the FDC disk change bit. In the XT mode, IDE7 is not used.
				MISCELLANEOUS
58	Power Good	PWRGD	I	FDC37C665IR (Motherboard Mode): This input indicates that the power (Vcc) is valid. For device operation, PWRGD must be active. When PWRGD is inactive, all inputs to the FDC37C665IR are disconnected and put in a low power mode, all outputs are put into high impedance. The contents of all registers are preserved as long as V_{CC} has a valid value. The driver current drain in this mode drops to ISTBY - standby current. This input has a weak pullup resistor to V_{CC}.
	Game Port Chip Select	GAMECS	O2	FDC37C666IR (Adapter Mode): This is the Game Port Chip Select output - active low. It will go active when the I/O address is 201H.
	Parallel Port Mode Control	PADCF	I	FDC37C666IR (Adapter Mode): Parallel Port Mode Control. Refer to FDC37C666IR hardware configuration for more information. Read and latched during reset active.
20	CLOCK 1	X1/CLK1	ICLK	The external connection for a parallel resonant 24 MHz crystal. A CMOS compatible oscillator is required if crystal is not used.
21	CLOCK 2	X2/CLK2	OCLK	24 MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers.
98	I/O Power	V_{IO}		I/O Interface supply pin (5 volt)
15, 72	Power	V_{CC}		+3.3 volt supply pin.
6, 47, 67, 95	Ground	GND		Ground pin.

Note 1: These active low open drain outputs select motor drives 0 ~ 3. In non-ECP modes, four drives can be supported directly. These motor enable bits are controlled by software via the Digital Output Register (DOR). In ECP mode, MTR0, 1 can be used to directly support 2 drives or can support 4 drives by using an external 2 to 4 decoder.

Note 2: Active low open drain outputs select drives 0 ~ 3. In non-ECP modes, four drives can BE supported directly. These drive select outputs are a decode of bits 0 and 1 of the Digital Output Register and qualified by the appropriate Motor Enable Bit of the DOR (bits 4 ~ 7). In ECP mode, DS0, 1 can be used to directly support 2 drives or can support 4 drives by using an external 2 to 4 decoder.

BUFFER TYPE DESCRIPTION

BUFFER TYPE	DESCRIPTION
I/O12	Input/output. 12 mA sink; 6 mA source
O12	Output. 12 mA sink; 6 mA source
OD20	Open drain. 20 mA sink
O2	Output. 2 mA sink; 1 mA source
O4	Output. 4 mA sink; 2.0 mA source
OD12	Output. 12 mA sink
OD12P	Open drain. 12 mA sink; 30μA source
OP12	Output. 12 mA sink; 6 mA source
OCLK	Output to external crystal
ICLK	Input to Crystal Oscillator Circuit (CMOS levels)
I	Input TTL compatible.
IS	Input with Schmitt Trigger.

9-1. FDD Controller

There is an FDC765A, Digital Data Separator, Write Precompensation and two FDC Peripheral Registers. It supports up to two floppy disk drivers. It is capable of either FM of MFM (includingdouble sided) recording, and will operate in either DMA or non-DMA mode.
In the non-DMA mode, the FDC generates an interrupt to the processor every time a data byte is to be transferred.
In DMA mode, the processor needs only to load the command into the FDC and all data transfers occur under the control of the FDC and DMA controllers respectively.
Pins of /MO0, /MO1, /DS0 and /DS1 control which disk drive is selected and which motor is enabled, and these 4 pins are controlled by port $3F2. Port $3F7 is used to set up the data transfer rate to250kB/s, 300kB/s or 500kB/s.

(1) Data Transfer Rate

Disk Drive	360kB	1.2MB		720kB	1.44MB	
Diskette	360kB	360kB	1.2MB	720kB	720kB	1.44MB
Data Transfer rate	250kB/s	300kB/s	500kB/s	250kB/s	300kB/s	500kB/s

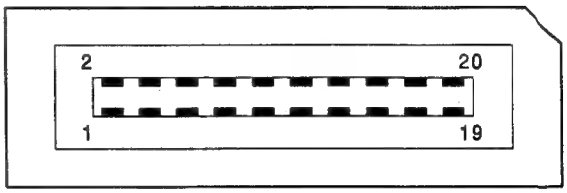
(2) FDC Registers

The are four registers used by the FDC and their functions are described in the following table.

Address Decoder		Data	Application (PC XT/AT)
Function	Port		
$\overline{IOW}$	$3F2	XD0 XD1 XD2 XD3 XD4 XD5 XD6 XD7	0-DRV:1-DRV1Reserved /Controller Reset INT/DRQ enabled Motor 0 enabled Motor 1 enabled Reserved Reserved
$\overline{IOR}$	$3F4		Decoded for 765A main Status Register
$\overline{IOR}$, $\overline{IOW}$	$3F5		Decoded for 765A Data Register
$\overline{IOR}$	$3F7	XD0-XD6 XD7	Reserved Diskette Change
$\overline{IOW}$	$3F7	XD0 XD1 XD2-XD7	0 1 0 0 0 1 Trans. rate 500 300 250 Reserved

For example, if write data #01h is written to port $3F7, then 300kB/s transfer rate will be selected. There is a built-in FDC 765A which executes 15 commands.
Port $3F4 and port $3F5 are decoded for 765A main status register (MSR) and data register (DR). The MSR contains the status information of the FDC, and may be accessed at any time.
The DR (which actually consists of several registers in a stack with only one register presented to the data bus at a time) stores data commands, parameters and FDD status information. Data bytes areread out of or written into the DR in order to program or obtain the results after a particular command. Therefore users can program FDC 765A via port $3F4 and $3F5.

FDD CON (CON13)



Pin	Signal	Pin	Signal
1	DCHG*	11	WG*
2	VCC (5V)	12	DIRC*
3	MD0*	13	GND
4	DS0*	14	WDD*
5	MS16*	15	GND
6	INDEX*	16	TR0*
7	FDD INSTALLED*	17	WP*
8	DSOUT*	18	GND
9	STEP*	19	RDD*
10	VCC (5V)	20	HS*

NOTE : MS16*, DSOUT* RESERVED FOR 3-MODE FDD

9-2. Serial Communication Port 1

Description

There are two independent UARTs, and they are fully compatible with NS 16550. The UART performs serial-to-parallel conversionon data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received tom the CPU. The CPU can read the complete status of the UART at any time during the operation.
Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions. In the TH6460, the programmable baud generator allows division of any input clock by 1 to generate the intenal 16X clock.
There are eleven registers in each UART (as shown below). They can be accessed via the CPU. These registers control UART operations including transmission and reception of data.

(1) Serial Port Registers

DLAB (LCR bit7)	COM1 Port	Register Symbol	Register Name
0	$3F8	RBR	Receive Bufffer Register, Read Only
0	$3F8	THR	Transmitter Holding Register, Write Only
0	$3F9	IER	Interrupt Enable Register
0	$3FA	IIR	Interrupt Identification Register
X	$3FB	LCR	Line Control Register
X	$3FC	MCR	Modem Control Register
X	$3FD	LSR	Line Status Register
X	$3FE	MSR	Modem Status Register
X	$3FF	SCR	Scratch Status Register
1	$3F8	DLL	Divisor Register
1	$3F9	DLM	Divisor Registor

(2) Serial Port Connector Assignment

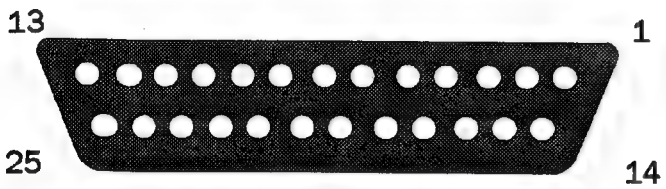
Pin	Symbol	Type	Description
1	$\overline{DCDA}$	I	Data carrier detect
2	SINA	I	Data input
3	SOITA	I/O	Data output
4	$\overline{DTRA}$	I/O	Data terminal ready
5	GEN		Signal ground
6	$\overline{DSRA}$	I	Data set ready
7	$\overline{RTSA}$	I/O	Request to send
8	$\overline{CTSA}$	I	Clear to send
9	$\overline{RIA}$	I	Ring indicate

Notes:

1. $\overline{\text{Indicates}}$ active low signal. Direction is with respect to the host.
2. I indicates to the host.
3. O indicates from the host.

9-3. Parallel Interface

(1) Printer Connector Pin Diagram



Parallel Port

(2) Connector Pin Assignment

Pin	Symbol	Type	Description
1	$\overline{STROBE}$	I/O	Printer strobe
2	PDB 0	I/O	Print data bit 0
3	PDB 1	I/O	Print data bit 1
4	PDB 2	I/O	Print data bit 2
5	PDB 3	I/O	Print data bit 3
6	PDB 4	I/O	Print data bit 4
7	PDB 5	O	Print data bit 5
8	PDB 6	O	Print data bit 6
9	PDB 7	O	Print data bit 7
10	$\overline{ACKG}$	I	Printer acknowledge
11	BUSY	I	Printer busy
12	PE	I	Out of paper
13	SLCT	I/O	Printer select
14	$\overline{ATF}$	I/O	Auto feed
15	$\overline{ERROR}$	I	Printer error
16	/INIT	I/O	Initialize printer
17	$\overline{SLCTIN}$	I/O	Select input
18-25	GND		Ground

Notes:

1. $\overline{\text{Indicates}}$ active low signal. Direction is with respect to the host.
2. I indicates to the host.
3. O indicates from the host.

10. FDD Drive (Canon MD3671)

10-1. Description

The Canon MD3671, 3.5-inch micro floppy disk drive is activated by 5 voltage-single power source and provides 2MB and 1MB unformatted storage capacity respectively. Signal connection between MD3671 and the system are made via 26pin FFC connector.

(1) Key Feature

- Compact drive
  Canon MD3671 is only 12.7mm beight, 101.6mm width, 101.6mm depth and it weighs only 120g. Its compactness is suitable for use in lap top or note book size computer systems.
- Compact DD motor
  The compact DDmotor produced by Canon's precision machinery technology allows an extremely compact drive, and ensures high reliability.

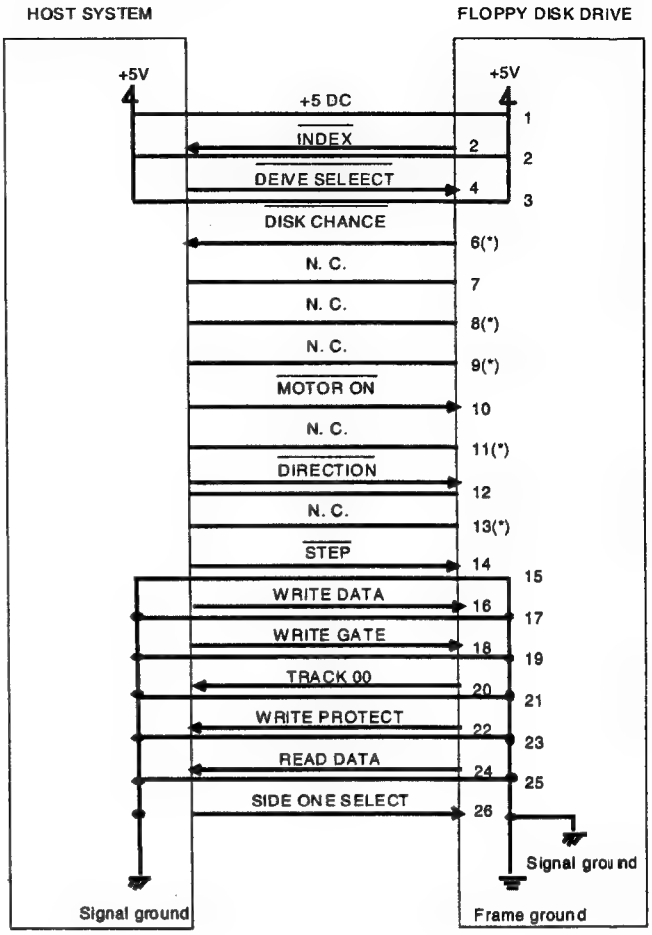
10-2. SPECIFICATIONS

ITEMS	MODE	2MB MODE	1MB MODE
Recording Capacity	Unformatted	2 MBytes	1MBytes
	Formatted	1474.6KbYTES	737.3KBytes
	Per Track	12.5KBytes	6.25KBytes
Data Transfer Rate		500 Kbits/sec.	250 Kbits/sec.
Recording Capacity Swiching System		Media Automatic Recognition.	
Access Time	Track to Track	3 msec. (min)	
	Seek Settling Time	15 msec.	
	Average Access Time	94 msec. (min)	
Disk Rotational Speed		300 rpm	
Average Latency		100 msec	
Spindle Motor Start Time		400 msec. (max)	
Recording Density at Innermost Track		1743 B.P.I.	8717 B.P.I.
Number of Tracks	Track Per Side	80	
	Track Per Disk	160	
Track Density		135 T.P.I.	
Number of Head		2	
Encoding Method		MFM	

Environmental Conditions	MODE / ITEMS	Operating	Non-operating	Transporting
	TEmperature	5°C45°C	-22°C55°C	-40°C62°C
	Humidity	20-80 %RH	10-90 %RH	5-90 %RH
	Maximum Wet Bulb Temperature	29°C	40°C	42°C
Vibration Resistance		0.5G	2G	2G
Shock Resistance		5G	100 G for 11 msec.	
D.C. Voltage Requirements		+5V±10%, Ripple; 100 mVp-p(DC to 1MHz)		
Power Consumption		Stand by ; 45 mW (TYP)		
		Operating ; 1.3 W (TYP)		
External View		12.7 mm(H)x101.6 mm(W)x101.6 (105.6)		
Weight		120 g (TYP)		
Bezel and Button Color		Black		
Activity LED		Green		
Reliability	MTBF	10,000 P.O.H		
	MTTR	30 min.		
	Unit Life	5 years		
	Soft Read Errors	Less than 10 -9 bits.		
	Hard Read Errors	Less than 10 -12 bits.		
	Seek Errors	Less than 10 -6 bits.		

10-3. INTERFACE

(1) Signal Interface



Signal Interface

*Optional Signal Lines.

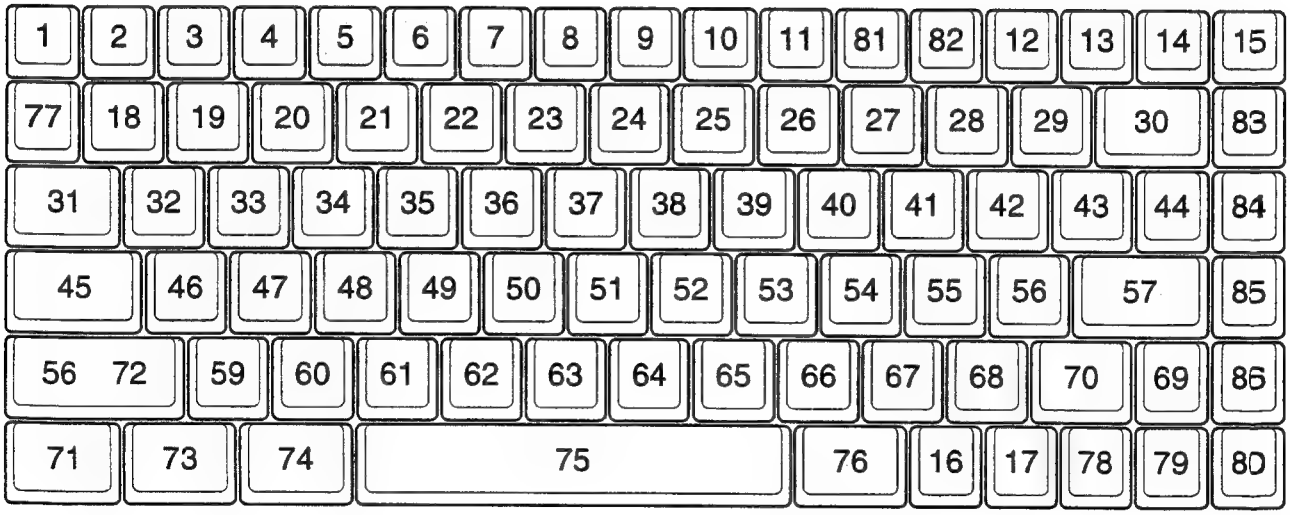
6 pin: DRIVE SELECT 1
8 pin: HD OUT or READY
9 pin: HD OUT
11pin: HD SEL. or LD SEL.
13 pin: DISK CHANGE or READY

11. Internal Key board (BTC-5004 Notebook keyboard)

11-1. Specification:

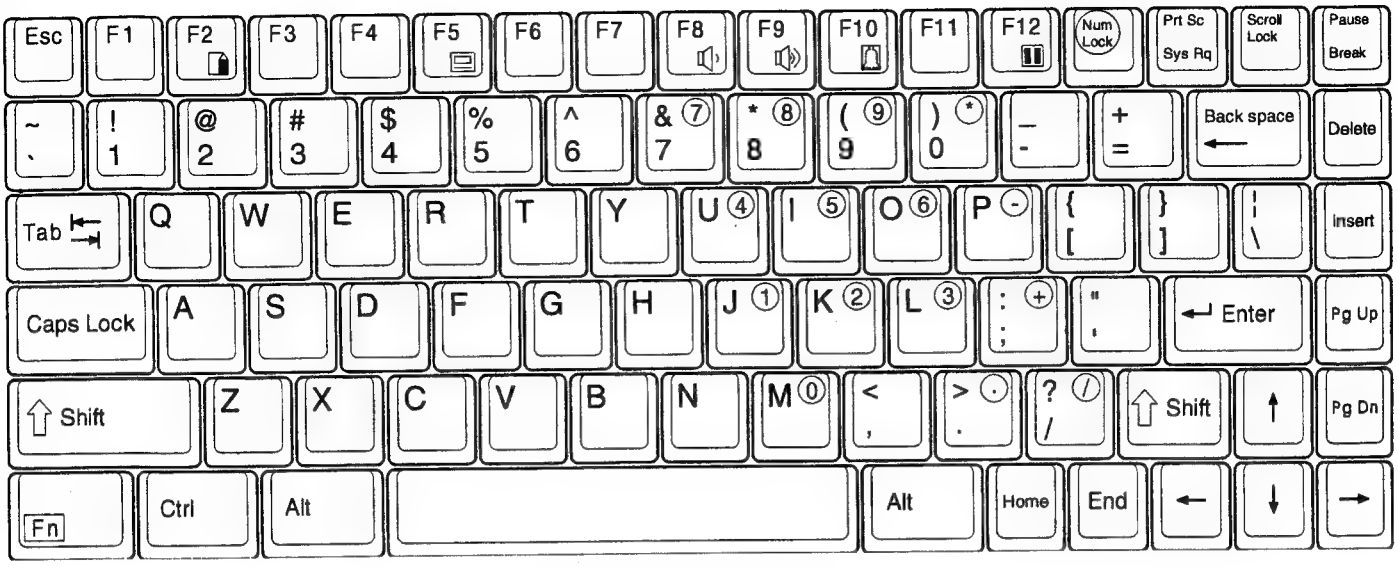
1. OUTSIDE DIMENSION: 278.45x114.8x10.2mm
2. KEY LAYOUT: SEE ATTACHED
3. TOTAL HEIGHT: 10.2 + /-0.2mm
4. KEY PITCH: 18.36mm
5. WEIGHT: 155 + /20g
6. SWITCH TYPE: CONDUCTIVE RUBBER
7. ACTUATION FORCE: 55 + /-15g
8. TRAVEL: 2.5 + /-0.2mm
9. CONTACT RESISTANCE: MAX 1kOHM
10. BOUNCE: MAX 15ms
11. LIFE: OVER 5 MILLION CYCLE
12. FN KEY
13. COMPATIBILITY: 85/86 KEY KEYBOARD COMPATIBLE WITH 101/102 AT AND PS/2 FUNCTION
14. KEYTOP LEGEND ENDURANCE: MEET CNS
15. EXTRACTION FORCE: 1.2g MIN.

(1) Key Position Numbers



KeyPosition Number

(2) Keyboard Layout (US)



Keyboard Layout (US English)

(3) Keyboard Matrix

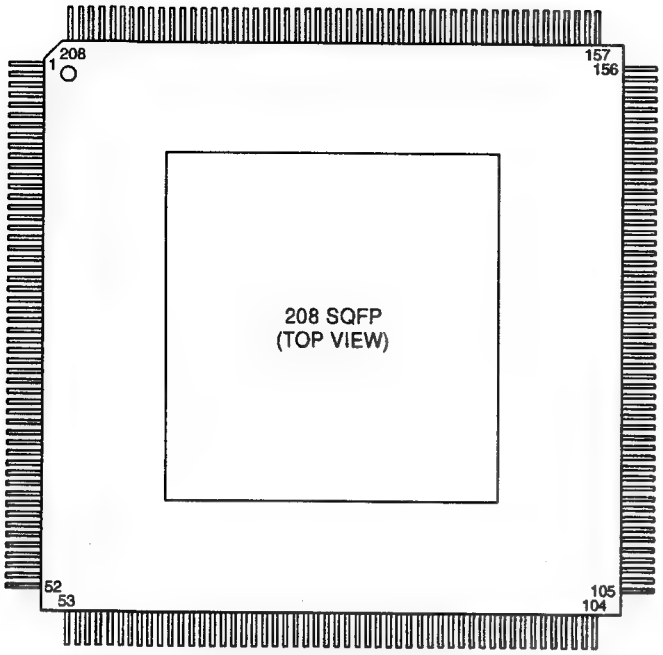
CON7

		R0	R1	R2	R3	R4	R5	R6	R7
1	S0			49	35	22	62	60	6
2	S1			50	36		63		7
3	S2		5	48	34	21	61	59	
4	S3	4		47	33	20		58	86
5	S4	3		46	32	19	73		
6	S5	2	74	45		18			
7	S6		72	51	37	23		85	8
8	S7	1	75		31	83	71	64	
9	S8		80	57	44	30	70	17	16
10	S9					84	69	79	15
11	S10				43	29	66	78	14
12	S11			56	42	28	67	77	13
13	S12			52	38	24	65		9
14	S13			53	39	27		76	12
15	S14			55	41	26	68	82	11
16	S15		87	54	40	25		81	10

1 2 3 4 5 6 7 8 CON10

Keyboard Matrix

12. WD90C24A/A2 VGA Controller



1. Host Interface Pin Definitions

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
71	$\overline{\text{IOCS16}}$	AT	Active Low Output	**I/O Chip Select 16 Bits** In AT mode, this signal used to respond to the host to allow 16-bit access to the I/O bus.
		PI	Active Low Output	**I/O Chip Select 16 Bits** In PI mode, since no 8-bit access will occur, this signal should be connected to VSS so it is always low.
	$\overline{\text{BOFF}}$	LOC	Active Low Output	**Bus Backoff** Connects to the 80486 BOFF pin. When active low, the 80486 retracts its last cycle and enables other masters to control the local bus. Its operation is similar to a read cycle for the VGA when the write buffers are full.
	$\overline{\text{CDSETUP}}$	MC	Active Low Input	**Card Setup** This signal is driven by the host to individually select channel connector slots during system configuration.
72	$\overline{\text{MEMCS16}}$	AT	Active Low Output	**Memory Chip Select 16 Bits** This line is used to respond to the host to enable 16-bit video memory data transfer.
	PM/$\overline{\text{IO}}$	PI	Active Low Input	**PI Bus Memory or I/O** Indicates the type of cycle currently executing on the PI bus. When high, the cycle is a memory operation, and when low the cycle is an Input/Output operation.
	PD31	LOC	Active High Input/Output	**CPU Data Bus Bit 32** Provides bit 32 on the Local bus. This bit is combined with PD30 (pin 75), PD29:PD16, and SD15:SD0 to provide a 32-bit Local Data bus.
	$\overline{\text{CDDS16}}$	MC	Active Low Output	**Card Data Size 16 Bits** Indicates that a 16-bit resource is available at the current address.
73	$\overline{\text{SBHE}}$	AT PI MC	Active Low Input	**System Byte High Enable** Indicates a data transfer on the upper byte of the data bus (SD 15:8).
	CPURESET	LOC	Active High Input	**CPU Reset** Local bus reset operation similar to AT bus RESET. This signal is used, primarily for the 386-based systems, to synchronize the divided-by-2 clock (internal working clock) on the Local Bus Interface between the WD90C24 and CPU. For 486-based systems this line should be tied low.

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
74	ALE	AT	Active High Input	**Address Latch Enable** Address bits SLA23:SLA17 are latched internally on the falling edge of the ALE.
	$\overline{\text{PSTART}}$	PI	Active Low Input	**PI Bus Start Signal** Indicates the start of a PI bus cycle. This signal is used to latch the address bus and command lines PM/$\overline{\text{IO}}$, PW/$\overline{\text{R}}$, and VGACS.
	$\overline{\text{ADS}}$	LOC	Active Low Input	**Address Status** Indicates the start of a Local bus cycle.
	$\overline{\text{ALD}}$	MC	Active Low Input	**Address Decode Latch** In MicroChannel mode, this signal is not used and the line should be tied to VSS (ground).
75	IRQ	AT	Active High Output	**Interrupt Request** Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. When the end of Vertical Display occurs, this signal goes active, causing an interrupt. It stays active until CRTC11 bit 4 clears it. In an AT system IRQ is usually not connected, but may be connected if desired.
	$\overline{\text{IRQ}}$	MC	Active Low Output	**Interrupt Request** Works similar to AT bus mode except that it is active low instead of active high.
	PD30	LOC	Active High Input/Output	**CPU Data Bus Bit 30** Provides bit 31 on the Local bus. This bit is combined with PD31 (pin 72), PD29:PD16, and SD15:SD0 to provide a 32-bit Local Data bus.
76	$\overline{\text{EIO}}$	AT	Active Low Input	**Enable I/O** This signal is used to enable I/O address decoding and is connected directly to the system bus signal $\overline{\text{AE}}$ (address enable).
	$\overline{\text{BE0}}$	LOC	Active Low Input	**Byte Enable 0** Byte enable for Local bus data bits SD7:SD0. $\overline{\text{BE3}}$:$\overline{\text{BE1}}$ are located on pins 80, 81, and 99, respectively.
	3C3D0	MC	Active High Input	**Video Subsystem Enable Port** When pulled high, this signal "wakes up" the WD90C24 in a manner identical to setting the Wakeup Register (3C3h) bit 0 to 1. This signal enables video subsystem memory and I/O address decoding.
77	$\overline{\text{IOCHRDY}}$	AT	Active Low Output	**Ready** Indicates to the system processor that a memory access is completed. It is used to add wait states to the CPU bus cycles during video memory accesses. It may be pulled inactive by the WD90C24 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.
	$\overline{\text{CPURDY}}$	LOC	Active Low Output, Open Collector	**CPU Ready** Ready signal to host processor or Local Bus controller for the termination of the current instruction cycles.
	$\overline{\text{CDCHRDY}}$	MC	Active Low Output	**Channel Ready** This signal is normally active, and is driven not active by the WD90C24 to allow additional time to complete a channel cycle.
78	$\overline{\text{ZWST}}$	AT	Active Low Output	**Zero Wait State** This signal can be used to generate zero wait states to the AT bus. This signal can be programmed by the PR33(A) register, bits 7.6 in the following ways: A. $\overline{\text{OWS}}$ = 0 if write cache is not full. B = $\overline{\text{OWS}}$ = 0 if valid memory address decode AND write cache is not full. In this case $\overline{\text{0WS}}$ = 0 should be ANDed externally with $\overline{\text{MWR}}$ to generate zero wait state strobe. C. $\overline{\text{0WS}}$ = 0 if valid memory address decode AND write cache is not full. AND $\overline{\text{MWR}}$ is active. D. $\overline{\text{0WS}}$ = 0 if valid memory address decode AND write cache is not full AND $\overline{\text{MWR}}$ is active, OR valid I/O address decode AND $\overline{\text{IOW}}$ is active.
	$\overline{\text{PCMD}}$	PI	Active Low Input	**PI Bus Cycle Command** When asserted during write cycles, this signal indicates valid data on the PI bus, or that data bytes are ready to read. This signal must be asserted during read cycles to provide an output enable.
	VLBIBUSY	LOC	Active High Output, Open Collector	**VGA Local Bus Busy Signal** Local bus interface busy signal.
	$\overline{\text{CSFB}}$	MC	Active Low Output, Open Collector	**Card Selected Feedback** Asserted by WD90C24 to acknowledge its selection. Cannot be asserted if $\overline{\text{CDSETUP}}$ is asserted.

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
98	$\overline{IOR}$	AT, PI	Active Low Input	**I/O Read** I/O read strobe. This strobe signals an I/O read.
	D/$\overline{C}$	LOC	Active Low Input	**Data or Code Indicator** Provides data or code indicator for the local bus.
	$\overline{S1}$	MC	Active Low Input	**S1 Cycle Decode** Microchannel status. Used with $\overline{S0}$, M/$\overline{IO}$, and $\overline{CMD}$ to decode Microchannel bus cycles.
99	$\overline{IOW}$	AT, PI	Active Low Input	**I/O Write** Active low write strobe. This strobe signals an I/O write.
	$\overline{BE1}$	LOC	Active Low Input	**Byte Enable 1** Byte enable for Local bus data bits SD15:SD8. $\overline{BE3}$, $\overline{BE2}$, and $\overline{BE0}$ are located on pins 80, 81, and 76, respectively.
	$\overline{CMD}$	MC	Active Low Input	**Command** Microchannel command. Used with $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO}$ to decode Microchannel bus cycles.
100	$\overline{MEMR}$	AT	Active Low Input	**Memory Read** This signal indicates that a memory read cycle is occurring. $\overline{MEMR}$ is internally gated with $\overline{REFRESH}$.
	M/$\overline{IO}$	LOC	Active High/Low Input	**Memory or I/O Cycle** Local bus indicator for memory or I/O cycle. Low indicates I/O cycle and high indicates memory cycle.
	M/$\overline{IO}$	MC	Active High/Low Input	**Memory or I/O Cycle** Microchannel memory or I/O cycle indicator. Low indicates I/O cycle: high indicates memory cycle. Used with $\overline{S0}$, $\overline{S1}$, and $\overline{CMD}$ to decode Microchannel bus cycles.
101	$\overline{MEMW}$	AT	Input	**Memory Write** This signal indicates that a memory write cycle is occurring. $\overline{MEMW}$ is internally gated with $\overline{REFRESH}$.
	PW/$\overline{R}$	PI	Active High/Low Input	**Write or Read Cycle** Indicates the type of access occurring on the PI bus. When high, the access is a write operation, and when low the access is a read operation.
	W/$\overline{R}$	LOC	Active High/Low Input	**Write or Read Cycle** Indicates the type of access occurring on the Local bus. When high, the access is a write operation, and when low the access is a read operation.
	$\overline{S0}$	MC	Active Low Input	**S0 Cycle Decode** Microchannel status. Used with $\overline{S1}$, M/$\overline{IO}$, and $\overline{CMD}$ to decode Microchannel bus cycles.
162	RESET	AT, PI	Active High Input	**Reset** This signal resets the WD90C24. MCLK and VCLK should be connected to WD90C24 in order for the WD90C24 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the Display Buffer Memory bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
	$\overline{SYSRES}$	LOC	Active Low Input	**System Reset** This signal resets the WD90C24. MCLK and VCLK should be connected to WD90C24 in order for the WD90C24 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the Display Buffer Memory bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK clock periods.
	CHRESET	MC	Active High Input	**Channel Reset** Microchannel reset operation similar to AT bus RESET.
166	$\overline{REFRESH}$	AT, PI, MC	Active Low Input	**DRAM Refresh** Initiates video buffer memory refresh. This signal must be inactive for memory reads or writes to occur.
	$\overline{RDYIN}$	LOC	Active Low Input	**Ready In**This signal is used for synchronizing the local bus with the host processor.
171	$\overline{EBROM}$	AT, MC	Active Low Output	**Enable BIOS ROM** This is an active low signal to enable BIOS ROM (C0000h ~ C7FFFh) if enabled by PR1 (0). A WRITE to WD90C24 internal I/O port address 46E8h causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
	HRQ	LOC	Active High Input	**Hold Request** Indicates that a System Bus Request was received via a REFRESH, DMA, or MASTER signal. The host CPU responds by relinquishing the bus and asserting HOLD ACKNOWLEDGE.

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
172	$\overline{\text{PRDY}}$	PI	Active Low Output	**Bus Ready** Terminates a PI-bus cycle. The PI bus default is not ready and a bus cycle continues until $\overline{\text{PRDY}}$ is asserted by holding it low until the rising edge of $\overline{\text{PCMD}}$. The bus cycles is also terminated if $\overline{\text{PRDY}}$ is not asserted within a programmed time-out interval.
	$\overline{\text{VLBICS}}$	LOC	Active Low Output, Tristate	**Video Local Bus Interface Chip Select** Local bus chip select. This line is driven low only if the current cycle requires service by the Local bus interface. Otherwise, the line is tristated.
153 152 151 150 149 148 147	SA31 SA30 SA29 SA28 SA27 SA26 SA25	LOC	Active High Input	**Host System Address Bus (SA31 ~ SA25)** These local address bits should be connected to the host CPU address bus. These bits are combined with SLA23:SLA17, SA24 and SA16:SA2 to provide a 30-bit Local Bus Address. Internal pullup resistors are provided on these pins.
146	SA24	LOC	Active High Input	**Host System Address Bus (SA24)** This bit is combined with SLA23:SLA17 and SA16:SA2 to provide a 30-bit Local Bus Address. An internal pullup resistor is provided on this pin.
	$\overline{\text{VGACS}}$	PI	Active Low Input	**VGA Chip Select** Indicates access to user-defined VGA memory address space. It is not asserted during I/O cycles.
69 68 67 66 65 64 63	SLA23 SLA22 SLA21 SLA20 SLA19 SLA18 SLA17	All	Active High Input	**Host System/Latchable Address Bus (SLA23:SLA27)** These address bits should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, these bits are combined with SA16:SA0 to provide a 24-bit address bus. For the Local bus interface, these bits are combined with SA31:SA24 and SA16:SA2 to provide a 30-bit Address Bus.
97 96 95 94 93 92 91 90 89 87 86 85 84 83 82	SA16 SA15 SA14 SA13 SA12 SA11 SA10 SA9 SA8 SA7 SA6 SA5 SA4 SA3 SA2	All	Active High Input	**Host System Address Bus (SA16 ~ SA2)** These address bits should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, these bits are combined with SLA23:SLA17, SA1, and SA0 to provide a 24-bit address bus. For the Local bus interface, these bits are combined with SA31:SA24 and SLA23:SLA17 to provide a 30-bit Address Bus.
81	SA1	AT, PI, MC	Active High Input	**High System Address Bus (SA1)** This address bit should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, this bit is combined with SLA23:SLA17, SA16:SA2, and SA0 to provide a 24-bit address bus.
	$\overline{\text{BE2}}$	LOC	Active Low Input	**Byte Enable 2** Local bus Byte Enable: for a 16-bit host CPU, $\overline{\text{BE2}}$ = SA1; for a 32-bit host CPU, $\overline{\text{BE2}}$ enables SD[23:16] $\overline{\text{BE3}}$, $\overline{\text{BE1}}$, and $\overline{\text{BE0}}$ are located on pins 80, 99 and 76 respectively.
80	SA0	AT, PI, MC	Active High Input	**Host System Address Bus (SA0)** This address bit should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, this bit is combined with SLA23:SLA17, SA16:SA2, and SA1 to provide a 24-bit address bus.
	$\overline{\text{BE3}}$	LOC	Active Low Input	**Byte Enable 3** Local bus Byte Enable: for a 16-bit host CPU, $\overline{\text{BE3}}$ is tied to an external pullup resistor; for a 32-bit host CPU, $\overline{\text{BE3}}$ enables SD[31:24] $\overline{\text{BE2}}$:$\overline{\text{BE0}}$ are located on pins 81, 99, and 76, respectively.

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
53 54 55 56 58 59 60 61 117 116 115 114 112 111 110 109	SD15 SD14 SD13 SD12 SD11 SD10 SD9 SD8 SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0	All	Active High Input/Output	**DATA BUS (SD15 ~ SD0)** These bidirectional signals may be connected directly to a local data bus requiring less than 8 mA of source/sink, or may be connected through two external buffers. One external buffer for SD15:8 and the other external buffer for SD7:SD0. For the AT, PI, and MC bus interfaces, these bits provide a 16-bit system data bus. For the Local bus, these bits are combined with PD31 (pin 72), PD30 (pin 75), and PD29:PD16 to provide a 32-bit data bus.
37 38 39 40 41 42 44 45 46 47 49 50 51 52	PD29 PD28 PD27 PD26 PD25 PD24 PD23 PD22 PD21 PD20 PD19 PD18 PD17 PD16	LOC	Active High Input/Output	**CPU Data Bus Bits (PD29:PD16)** Provide bits 29:16 on the WD909C24 Local bus. These bits are combined with PD30 (pin 75), PD31 (pin 72), and SD15:SD0 to provide a 32-bit Local Data bus.
163	$\overline{\text{PDOWN}}$	All	Active Low Input	**Power Down Selected** This active low input signal is used to disable the screen refresh cycle. This pin has an internal 100 KOhm pullup resistor.

2. Display Buffer Memory Interface Pins

The display buffer memory interface is designed for connection of up to four 256Kx4 or one 256Kx16 fast-page-mode DRAMs. Also, memory data lines AMD[15:0] and BMD[15:0] are used to input configuration data (CNF[31:0]) at system power up and reset. For additional information on configuration bits, refer to the WD90C24 Configuration Register description.
This section is divided into the following subsections, which list the bus lines as follows:

- Bank A Video Memory Bus
- Bank B Video Memory Bus

2.1 Bank A Video Memory Bus (Bank A Video Memory Signals)

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
			BANK A VIDEO MEMORY DATA/CONFIGURATION BITS
178	AMD15	I/O	Bank A Memory Data Bit 15:Configuration Bit CNF15
180	AMD14	I/O	Bank A Memory Data Bit 14:Configuration Bit CNF14
182	AMD13	I/O	Bank A Memory Data Bit 13:Configuration Bit CNF13
184	AMD12	I/O	Bank A Memory Data Bit 12:Configuration Bit CNF12
186	AMD11	I/O	Bank A Memory Data Bit 11:Configuration Bit CNF8
188	AMD10	I/O	Bank A Memory Data Bit 10:Configuration Bit CNF10
190	AMD9	I/O	Bank A Memory Data Bit 9:Configuration Bit CNF9
192	AMD8	I/O	Bank A Memory Data Bit 8:Configuration Bit CNF11
191	AMD7	I/O	Bank A Memory Data Bit 7:Configuration Bit CNF7
189	AMD6	I/O	Bank A Memory Data Bit 6:Configuration Bit CNF6
187	AMD5	I/O	Bank A Memory Data Bit 5:Configuration Bit CNF5
185	AMD4	I/O	Bank A Memory Data Bit 4:Configuration Bit CNF4
183	AMD3	I/O	Bank A Memory Data Bit 3:Configuration Bit CNF3
181	AMD2	I/O	Bank A Memory Data Bit 2:Configuration Bit CNF2
179	AMD1	I/O	Bank A Memory Data Bit 1:Configuration Bit CNF1
177	AMD0	I/O	Bank A Memory Data Bit 0:Configuration Bit CNF0
NOTE:	AMD15 through AMD0 have internal 100 KOhm pullup resistors.		
			BANK A VIDEO MEMORY ADDRESS BITS
200	AMA8	Output	Bank A Memory Address Bit 8
	$\overline{\text{AWEL}}$	Active Low Output	**Write Enable Low Bank A** Write Enable control for video memory buffer DRAM bank A. This signal is used in memory configurations CNF4 and CNF5.
202	AMA7	Output	Bank A Memory Address Bit 7
204	AMA6	Output	Bank A Memory Address Bit 6
206	AMA5	Output	Bank A Memory Address Bit 5
208	AMA4	Output	Bank A Memory Address Bit 4
207	AMA3	Output	Bank A Memory Address Bit 3
205	AMA2	Output	Bank A Memory Address Bit 2
203	AMA1	Output	Bank A Memory Address Bit 1
201	AMA0	Output	Bank A Memory Address Bit 0
NOTE:	AMA8 through AMA0 form the primary 9-bit video buffer DRAM address bus. AMA8 is the MSB and AMA0 the LSB.		
			BANK A VIDEO MEMORY CONTROL LINES
194	$\overline{\text{ACASL}}$	Active Low Output	**CAS Bank A Low** Lower column address strobe for video memory buffer DRAM bank A.
196	$\overline{\text{AWE}}$	Active Low Output	**Write Enable Bank A** Write Enable control for video memory buffer DRAM bank A. When a 256Kx16 DRAM is used this is the DRAM write enable output.
	$\overline{\text{AWER}}$		**Write Enable High Bank A** Write Enable control for video memory buffer DRAM bank A. This signal is used in memory configurations CNF4 and CNF5.
197	$\overline{\text{ACASH}}$	Active Low Output	**CAS Bank A High** Upper column address strobe for video memory buffer DRAM bank A.
198	$\overline{\text{ARAS}}$	Active Low Output	**RAS Bank A** Row address strobe for video memory buffer DRAM bank A.
199	$\overline{\text{AOE}}$	Active Low Output	**Output Enable Bank A** Output Enable control for video memory buffer DRAM bank A. When a 256Kx16 DRAM is used, this is the DRAM output enable strobe.

2.2 Bank B Video Memory Bus (Bank B Video Memory Signals)

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
BANK B VIDEO MEMORY DATA BITS/CONFIGURATION BITS			
2	BMD15	I/O	Bank B Memory Data Bit 15:Configuration Bit CNF31
4	BMD14	I/O	Bank B Memory Data Bit 14:Configuration Bit CNF30
7	BMD13	I/O	Bank B Memory Data Bit 13:Configuration Bit CNF29
9	BMD12	I/O	Bank B Memory Data Bit 12:Configuration Bit CNF28
12	BMD11	I/O	Bank B Memory Data Bit 11:Configuration Bit CNF27
14	BMD10	I/O	Bank B Memory Data Bit 10:Configuration Bit CNF26
16	BMD9	I/O	Bank B Memory Data Bit 9:Configuration Bit CNF25
18	BMD8	I/O	Bank B Memory Data Bit 8:Configuration Bit CNF24
17	BMD7	I/O	Bank B Memory Data Bit 7:Configuration Bit CNF23
15	BMD6	I/O	Bank B Memory Data Bit 6:Configuration Bit CNF22
13	BMD5	I/O	Bank B Memory Data Bit 5:Configuration Bit CNF21
11	BMD4	I/O	Bank B Memory Data Bit 4:Configuration Bit CNF20
8	BMD3	I/O	Bank B Memory Data Bit 3:Configuration Bit CNF19
6	BMD2	I/O	Bank B Memory Data Bit 2:Configuration Bit CNF18
3	BMD1	I/O	Bank B Memory Data Bit 1:Configuration Bit CNF17
1	BMD0	I/O	Bank B Memory Data Bit 0:Configuration Bit CNF16
NOTE:	BMD15 through BMD0 have internal 100 KOhm pullup resistors.		
BANK B VIDEO MEMORY ADDRESS BITS			
27	BMA8	Output	Bank Memory Address Bit 8
	$\overline{\text{BWEL}}$	Active Low Output	**Write Enable Low Bank B** Write Enable control for video memory buffer DRAM bank B. This signal is used in memory configurations CNF3, CNF4, and CNF5.
29	BMA7	Output	Bank B Memory Address Bit 7
31	BMA6	Output	Bank B Memory Address Bit 6
33	BMA5	Output	Bank B Memory Address Bit 5
35	BMA4	Output	Bank B Memory Address Bit 4
34	BMA3	Output	Bank B Memory Address Bit 3
32	BMA2	Output	Bank B Memory Address Bit 2
30	BMA1	Output	Bank B Memory Address Bit 1
28	BMA0	Output	Bank B Memory Address Bit 0
BANK B VIDEO MEMORY ADDRESS CONTROL LINES			
20	$\overline{\text{BCASL}}$	Active Low Output	**CAS Bank B Low** Lower column address strobe for video memory buffer DRAM bank B.
22	$\overline{\text{BWE}}$	Active Low Output	**Write Enable Bank B** Write Enable control for video memory buffer DRAM bank B.
	$\overline{\text{BWER}}$		**Write Enable High Bank B** Write Enable control for video memory buffer DRAM bank B. This signal is used in memory configurations CNF3, CNF4, and CNF5.
23	$\overline{\text{BCASH}}$	Active Low Output	**CAS Bank B High** Upper column address strobe for video memory buffer DRAM bank B.
24	$\overline{\text{BRAS}}$	Active Low Output	**RAS Bank B** Row address strobe for video memory buffer DRAM bank B.
25	$\overline{\text{BOE}}$	Active Low Output	**Output Enable Bank B** Output Enable control for video memory buffer DRAM bank B.

3. RAM DAC/CRT Interface Pins

Internal DAC interface pins are described in the following table.

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
155	FSADJ	Analog Input	**Full Scale Adjust** A resistor (RSET) on this pin sets the full scale output current of the RED, GREEN, and BLUE DACs. FSADJ if pin 155 is above VSS. CAUTION: Do not ground this pin.
	$\overline{\text{MDETECT}}$	Active Low Input	**Monitor Detect** When pin 155 is grounded, this pin is used as a monitor detect input. The result of this input is read from 3C2h bit 4. $\overline{\text{MDETECT}}$ if pin 155 is tied to VSS.
156	VREF	Analog Input	**Voltage Reference Input** An external voltage reference of 1.2V is connected to this input for normal operation of the internal RAMDAC.
157	BLUE	Analog Output	**Blue Current Output** High impedance current source can directly drive a double-terminated 75-Ohm coaxial cable.
158	GREEN	Analog Output	**Green Current Output** High impedance current source can directly drive a double-terminated 75-Ohm coaxial cable.
159	RED	Analog Output	**Red Current Output** High impedance current source can directly drive a double-terminated 75-Ohm coaxial cable.
173	VSYNC	Active High Output	**CRT Vertical Sync** VSYNC is the CRT vertical sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable. Control of vertical sync polarity is done by setting register bits in the VGA Miscellaneous Output Register.
174	HSYNC	Active High Output	**CRT Horizontal Sync** HSYNC is the CRT horizontal sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable as is its position and duration. Control of horizontal sync polarity is done by setting register bits in the VGA Miscellaneous Output Register.
175	PCLK	Active High Input/Output	**Pixel Clock** Video pixel clock output used by the external RAMDAC to latch pixel data from the WD90C24 controller's video output bus into an external RAMDAC or panel interface. Pixel data from the WD90C24 changes on the rising edge of PCLK and is intended to be latched into an external RAMDAC or panel interface by the falling edge of PCLK. In Auxiliary Video Extender (AVE) Mode, this pin provides the input for the internal RAMDAC PCLK signal.

INTERNAL DAC INTERFACE PINS

4. Clock Generation Interface Pins

Clock generation interface pins are described in the following table.

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
70	CLK486	Input	**CPU Clock** Provides the clock input for the Local bus. This pin has an internal 100 KOhm pulldown resistor.
103	XMCLK	Input	**External Master Clock** In external clock mode, this signal is the MCLK input.
104	MCAP	Analog Input	**Analog Input** Connects to discrete filter network.
105	VCAP	Analog Input	**Analog Input** Connects to discrete filter network.
106	VCLK2	Input/Output	**Video Clock 2** In external clock mode, VCLK2 is one of three possible video clock inputs to the WD90C24. The three clock inputs (VCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types.
161	EXCKEN	Active High Input	**External Clock Enable** Asserted to select external clock mode
168	VCLK1	Input/Output	**Video Clock 1** In external clock mode, VCLK1 is one of three possible video clock inputs to the WD90C24. The three clock inputs (VCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types.
	FPUSR1	Output	**User Programmable Output 1** This line is a panel interface signal that can be programmed by the user to initiate or confirm an action. NOTE: In internal PCLK mode, VCLK1 is an output configured as FPUSR1
170	CKIN	Input	**System Clock Input** In internal PCLK mode, CKIN provides the CPU clock (14.318 MHz), which is the default mode. This pin has an internal 100 KOhm pulldown resistor.
	VCLK	Input	**External Video Clock** In external clock mode, VCLK is one of three possible video clock inputs to the WD90C24. The three clock inputs (VCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types.

CLOCK GENERATION INTERFACE PIN TABLE

Panel Interface Pins

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
119	XSCLKL	Active High Output	**External Shift Clock Lower** Used for 8-bit STN Color LCD (Seiko)
	XSCLKU		**External Shift Clock Upper** Used for 8-bit STN color LCD (Sharp)
	RGB17		**Red Green Blue Bit 17** Data bit 17 for 18-bit TFT color LCD
120	$\overline{\text{WPLT}}$	Active Low Output	**Write Palette** If the WD90C24 has been configured for external DAC mode, $\overline{\text{WPLT}}$ is the write pulse to the external RAMDAC or equivalent circuit.
	RGB16	Active High Output	**Red Green Blue Bit 16** Data bit 16 for 18-bit TFT color LCD
121	$\overline{\text{RPLT}}$	Active Low Output	**Read Palette** If not configured for a color TFT interface, this pin is the active low read pulse to the external RAMDAC or equivalent circuit.
	RGB15	Active High Output	**Red Green Blue Bit 15** Data bit 15 for 18-bit TFT color LCD
	STN15		**Super Twisted Nematic Bit 15** Data bit 15 for 16-bit STN color LCD
	BD3		**Blue Data Bit 3** Data Bit 3 for 9-bit and 12-bit TFT color LCD
	VD7		**Video Data Bit 7** Data bit 7 for the upper 8-bits of a 16-bit STN color interface

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
122	RGB14	Active High Output	**Red Green Blue Bit 14** Data bit 14 for 18-bit TFT color LCD
	STN14		**Super Twisted Nematic Bit 14** Data bit 14 for 16-bit STN color LCD
	BD2		**Blue Data Bit 2** Data Bit 0 for 9-bit and 12-bit TFT color LCD
	VD6		**Video Data Bit 6** Data bit 6 for the upper 8-bits of a 16-bit STN color interface
123	RGB13	Active High Output	**Red Green Blue Bit 13** Data bit 13 for 18-bit TFT color LCD
	STN13		**Super Twisted Nematic Bit 13** Data bit 13 for 16-bit STN color LCD
	BD1		**Blue Data Bit 1** Data Bit 1 for 9-bit and 12-bit TFT color LCD
	VD5		**Video Data Bit 5** Data bit 5 for the upper 8-bits of a 16-bit STN color interface
124	RGB12	Active High Output	**Red Green Blue Bit 12** Data bit 12 for 18-bit TFT color LCD
	STN12		**Super Twisted Nematic Bit 12** Data bit 12 for 16-bit STN color LCD
	BD0		**Blue Data Bit 0** Data Bit 0 for 3-bit, 9-bit, and 12-bit TFT color LCD
	VD4		**Video Data Bit 4** Data bit 4 for the upper 8-bits of a 16-bit STN color interface
126	RGB0	Active High Output	**Red Green Blue Bit 0** Data bit 0 for 18-bit TFT color LCD
	STN11		**Super Twisted Nematic Bit 11** Data bit 11 for 16-bit STN color LCD
	VD3		**Video Data Bit 3** Data bit 3 for the upper 8-bits of a 16-bit STN color interface
127	RGB1	Active High Output	**Red Green Blue Bit 1** Data bit 1 for 18-bit TFT color LCD
	STN10		**Super Twisted Nematic Bit 10** Data bit 10 for 16-bit STN color LCD
	VD2		**Video Data Bit 2** Data bit 2 for the upper 8-bits of a 16-bit STN color interface
128	RGB2	Active High Output	**Red Green Blue Bit 2** Data bit 2 for 18-bit TFT color LCD
	STN9		**Super Twisted Nematic Bit 9** Data bit 9 for 16-bit STN color LCD
	VD1		**Video Data Bit 1** Data bit 1 for the upper 8-bits of a 16-bit STN color interface
129	RGB3	Active High Output	**Red Green Blue Bit 3** Data bit 3 for 18-bit TFT color LCD
	STN8		**Super Twisted Nematic Bit 8** Data bit 8 for 16-bit STN color LCD
	VD0		**Video Data Bit 0** Data bit 0 for the upper 8-bits of a 16-bit STN color interface

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
131	RGB11	Active High Output	**Red Green Blue Bit 11** Data bit 11 for 18-bit TFT color LCD
	RD3		**Red Data Bit 3** Data bit 3 for 12-bit TFT color LCD
	STN7		**Super Twisted Nematic Bit 7** Data bit 7 for 8-bit and 16-bit STN color LCD
	LD7		**Video Lower Data Bit 7** Data bit 7 for the lower 8-bits of a 16-bit STN color interface
	VD7		**Video Data Bit 7** Data bit 7 for the 8-bit CRT interface
	VUD3		**UPPER PANEL DATA BIT 3** In a dual-panel LCD interface, VUD3 through VUD0 are used for the upper panel data bus. In a signal-panel LCD interface these pins also provide video data to the panel. In a plasma interface, they provide the pure 4-bit video data interface. In a CRT interface, they are the upper four bits of pixel video outputs to the RAMDAC. First Pixel VUD3 Pin 131 Second Pixel VUD2 Pin 132 Third Pixel VUD1 Pin 133 Fourth Pixel VUD0 Pin 134 In Auxiliary Video Extender (AVE) Mode, this pin provides the P7 input for the internal RAMDAC.
132	RGB10	Active High Output	**Red Green Blue Bit 10** Data bit 10 for 18-bit TFT color LCD.
	RD2		**Red Data Bit 2** Data bit 2 for 9-bit and 12-bit TFT color LCD
	STN6		**Super Twisted Nematic Bit 6** Data bit 6 for 8-bit and 16-bit STN color LCD
	LD6		**Video Lower Data Bit 6** Data bit 6 for the lower 8-bits of a 16-bit STN color interface.
	VD6		**Video Data Bit 6** Data bit 6 for the 8-bit CRT interface
	VUD2		**Upper Panel Data Bit 2** Refer to VUD3, pin 131 In Auxiliary Video Extender (AVE) Mode, this pin provides the P6 input for the internal RAMDAC.
133	RGB9	Active High Output	**Red Green Blue Bit 9** Data bit 9 for 18-bit TFT color LCD.
	RD1		**Red Data Bit 1** Data bit 1 for 9-bit and 12-bit TFT color LCD
	STN5		**Super Twisted Nematic Bit 5** Data bit 5 for 8-bit and 16-bit STN color LCD
	LD5		**Video Lower Data Bit 5** Data bit 5 for the lower 8-bits of a 16-bit STN color interface
	VD5		**Video Data Bit 5** Data bit 5 for the 8-bit CRT interface
	VUD1		**Upper Panel Data Bit 1** Refer to VUD3, pin 131 In Auxiliary Video Extender (AVE) Mode, this pin provides the P5 input for the internal RAMDAC.
134	RGB8	Active High Output	**Red Green Blue Bit 8** Data bit 8 for 18-bit TFT color LCD.
	RD0		**Red Data Bit 0** Data Bit 0 for 3-bit, 9-bit, and 12-bit TFT color LCD
	STN4		**Super Twisted Nematic Bit 4** Data bit 4 for 8-bit and 16-bit STN color LCD
	LD4		**Video Lower Data Bit 4** Data bit 4 for the lower 8-bits of a 16-bit STN color interface
	VD4		**Video Data Bit 4** Data bit 4 for the 8-bit CRT interface
	VUD0		**Upper Panel Data Bit 0** Refer to VUD3, pin 131 In Auxiliary Video Extender (AVE) Mode, this pin provides the P4 input for the internal RAMDAC.

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
135	RGB7	Active High Output	**Red Green Blue Bit 17** Data bit 17 for 18-bit TFT color LCD.
	GD3		**Green Data Bit 3** Data bit 3 for 12-bit TFT color LCD
	STN3		**Super Twisted Nematic Bit 3** Data bit 3 for 8-bit and 16-bit STN color LCD
	LD3		**Video Lower Data Bit 3** Data bit 3 for the lower 8-bits of a 16-bit STN color interface
	VD3		**Video Data Bit 7** Data bit 7 for the 8-bit CRT interface
	VLD3		**Lower Panel Data Bit 3** In a dual-panel LCD interface, VLD3 through VLD0 are used for the lower panel data bus. In a 4-bit plasma interface, they are reserved. In an 8-bit plasma interface they provide the second pixel of video data to the panel. In a CRT interface, they are the lower four bits of pixel video outputs to the RAMDAC. In Auxiliary Video Extender (AVE) Mode, this pin provides the P3 input for the internal RAMDAC.
136	RGB6	Active High Output	**Red Green Blue Bit 6** Data bit 6 for 18-bit TFT color LCD.
	GD2		**Green Data Bit 2** Data bit 2 for 9-bit and 12-bit TFT color LCD
	STN2		**Super Twisted Nematic Bit 2** Data bit 2 for 8-bit and 16-bit STN color LCD
	LD2		**Video Lower Data Bit 2** Data bit 2 for the lower 8-bits of a 16-bit STN color interface
	VD2		**Video Data Bit 2** Data bit 2 for the 8-bit CRT interface
	VLD2		**Lower Panel Data Bit 2** Refer to VLD3, pin 135 In Auxiliary Video Extender (AVE) Mode, this pin provides the P2 input for the internal RAMDAC.
137	RGB5	Active High Output	**Red Green Blue Bit 5** Data bit 5 for 18-bit TFT color LCD.
	GD1		**Green Data Bit 1** Data bit 1 for 9-bit and 12-bit TFT color LCD
	GD0		**Green Data Bit 0** Data bit 0 for 3-bit TFT color LCD
	STN1		**Super Twisted Nematic Bit 1** Data bit 1 for 8-bit and 16-bit STN color LCD
	LD1		**Video Lower Data Bit 1** Data bit 1 for the lower 8-bits of a 16-bit STN color interface
	VD1		**Video Data Bit 1** Data bit 1 for the 8-bit CRT interface
	VLD1		**Lower Panel Data Bit 1** Refer to VLD3, pin 135 In Auxiliary video Extender (AVE) Mode, this pin provides the P1 input for the internal RAMDAC.
138	RGB4	Active High Output	**Red Green Blue Bit 4** Data bit 4 for 18-bit TFT color LCD.
	GD0		**Green Data Bit 0** Data bit 0 for 9-bit and 12-bit TFT color LCD
	STN0		**Super Twisted Nematic Bit 0** Data bit 0 for 8-bit and 16-bit STN color LCD
	LD0		**Video Lower Data Bit 0** Data bit 0 for the lower 8-bits of a 16-bit STN color interface
	VD0		**Video Data Bit 0** Data bit 0 for the 8-bit CRT interface
	VLD0		**Lower Panel Data Bit 0** Refer to VLD3, pin 135 In Auxiliary Video Extender (AVE) Mode, this pin provides the P0 input for the internal RAMDAC.

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
140	XSCLK	Active High Output	**X Driver Shift Clock** In a single panel interface, this signal is used to shift the data into the X-driver.
	XSCLKL		**External Shift Clock Lower** Used for 8-bit STN color LCD (Sharp)
	XSCLKU		**External Shift Clock Upper** Used for 8-bit STN color LCD (Seiko)
	SCLK		**Shift Clock** In a single panel interface, this signal is used to shift the upper and lower panel data into the display drivers.
142	LP	Active High Output	**Latch Pulse** The LP output is intended to be used by a panel to latch all the current panel data into the current scan line of the panel.
143	FP	Active High Output	**Frame Pulse** FP is output as an indication to attached panels that a frame has begun.
144	FR	Active High Output	**Frame Rate Signal** Whenever the WD90C24 is operating in any LCD mode, FR is a free-running clock, which is intended to be connected to FR inputs on some LCD panels. Frequency of its signal is programmable and is controlled by setting PR62.
	$\overline{\text{BLANK}}$	Active Low Input/Output	**Blanking Control Signal** BLANK is the standard analog VGA RAMDAC blanking signal. Output when the WD90C24 is not operating in any LCD modes. In Auxiliary video Extender (AVE) Mode, this pin provides the $\overline{\text{BLANK}}$ input for the internal RAMDAC.
	ENDATA	Active High Output	**Enable Data** This is a data enable output for panels. In a plasma interface, it is an "enable video" signal.
164	$\overline{\text{LCDENA}}$	Active Low Output	**LCD Panel Enable** $\overline{\text{LCDENA}}$ is used to control the power supply for the attached panel.
165	PNLOFF	Active High Output	**Panel Power Off** Provides the power off signal to the bias supply circuit of an LCD panel. The PNLOFF signal is used as a power enable/disable to the high voltage bias inverter of a panel, and is tied to the WD90C24 controller's power management circuit. The WD90C24 sequences this signal as part of the panel power-on/power-off procedures designed to protect panel power circuit. A high at this output indicates power-off to the panel and a low power-on.
167	FPUSR0	Output	**User Programmable Output 0** This line can be programmed by the user to initiate or confirm an action.
168	FPUSR1	Output	**User Programmable Output 1** This line can be programmed by the user to initiate or confirm an action. NOTE: In external PCLK mode, FPUSR1 is configured as VCLK1.

6. Power and Ground Pins

PIN NO.	MNEMONIC	DESCRIPTION
5, 21, 36, 48, 62, 79, 118, 139, 176, 195	VSS	Ground VSS=0V
10, 26, 43, 125	VDD	Main VDD Power to Core Logic
19, 193	MVDD	Memory Interface VDD Supply
57, 113	BVDD	System Bus Interface VDD Supply
88, 141	RVDD	RAM Filtered Palette VDD Supply
102	AVDD1	PCLK Analog Power
107	AVSS1	PCLK Analog Ground
108, 145	RVSS	RAM Palette VSS Ground
130	FPVDD	Panel Interface VDD Supply
154	AVDD2	RAMDAC Analog Power
160	AVSS2	RAMDAC Analog Ground
169	PVDD	Power-Down Section VDD Supply

POWER AND GROUND SIGNAL DEFINITIONS

13. LCD UNIT AND LCD CONTROLLER

1. Application

This specification applies to color TFT-LCD module. LQ9D021.
CCFT is SINGLE LAMP TYPE.

2. Overview

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, control circuit and power supply circuit and a backlight unit. Graphics and texts can be displayed on a 640x3x480 dots panel in 512 colors by supplying 9 bit data signal, four kinds of timing signals, +5V DC supply voltage for TFT-LCD panel driving and supply voltage for backlight. Optimum viewing angle direction is 6 o'clock.
400 lines and 350 lines modes in addition to the 480 lines mode can be also applied for this module.

Backlight-driving DC/AC inverter is not built in this module.

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen size	8.4 (Diagonal)	inch
Effective display area	170.9(H) x 129.6(V)	mm
Display pixels	640(H) x 480(V)	pixel
	(1 pixel=R+G+B dots)	
Pixel pitch	0.267(H) x 0.270(V)	mm
Pixel configuration	R, G, B vertical stripe	
Display mode	Normally white	
Unit outline dimensions *1	242.5(W)x179.2(H)x8.7(D)	mm
Weight	485±20	g
Surface treatment	anti-glare and hard-coating 2H	

*1. Note: excluding backlight cables.

Outline dimensions is shown in Fig. 1

4. Input Terminals

4-1) TFT-LCD panel driving

CN1 (Interface signal)

Used connector: DF9B-31P-1V (Hirose Electric Co., Ltd.)
Corresponding connector: DF9B-31S-1V (Hirose Electric Co., Ltd.)

Pin No.	Symbol	Function	Remark
1	TST	This should be electrically opened during operation	
2	GND		
3	R0	RED data signal (LSB)	
4	Vsync	vertical sync signal	[Note1]
5	R1	RED data signal	
6	Hsync	Horizontal sync signal	[Note1]
7	R2	RED Data signal (MSB)	
8	GND		
9	GND		
10	CK	Clock signal for sampling each data signal	
11	TST	This should be electrically opened during operation	
12	GND		
13	G0	GREEN Data signal (LSB)	
14	TST	This should be electrically opened during operation	
15	GND		
16	TST	This should be electrically opened during operation	
17	G1	GREEN Data signal	
18	TST	This should be electrically opened during operation	
19	G2	GREEN data signal (MSB)	
20	GND		
21	GND		
22	VCC	+5V power supply	
23	TST	This should be electrically opened during operation	
24	VCC	+5V power supply	
25	B0	BLUE data signal (LSB)	
26	TST	This should be electrically opened during operation	
27	GND		
28	ENAB	Data enable signal (to settle the viewing area)	
29	B1	BLUE data signal	
30	GND		
31	B2	Blue data signal (MSB)	

[Note1] Polarity of the sync. signals.

mode	480 lines	300 lines	350 lines
Hsync	negative	negative	positive
Vsync	negative	positive	negative

* The shielding case is connected with GND.

4-2) Backlight

CNA

Used connector : BHR-03VS-1(JST)
Corresponding connector : SM02(8.0)B-BHS(JST)

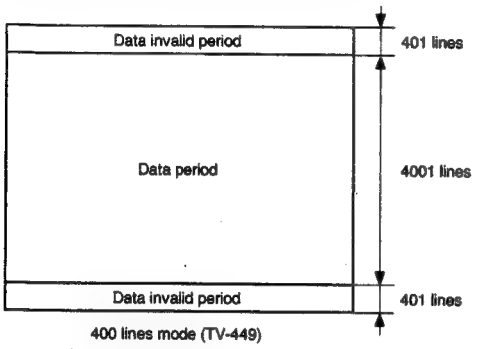
Pin no.	symbol	function
1	V_{HIGH}	Power supply for lamp (High voltage side)
3	V_{LOW}	Power supply for lamp (Low voltage side)

6-2-c) Vertical display position

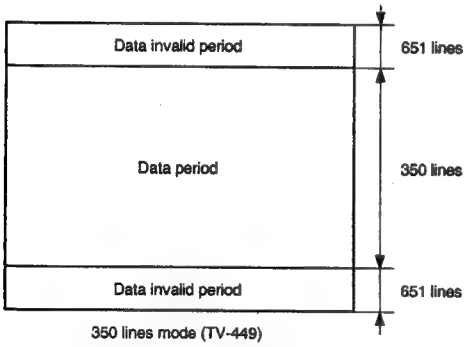
The vertical display position is centered in 480 line and 350 line modes of VGA with the polarity of the sync. signals and values in the following table. The data enable signal doesn't effect the vertical display position.

mode	V-data start(TVs)	V-data period(TVd)	V-display start	V-display period	Unit	Remark
480	34	480	34	480	line	
400	34	400	443-TV	480	line	[Note1]
350	61	350	445-TV	480	line	

[Note1] Since during vertical data invalid period is displayed in 400 and 350 line modes, inputting all data "0" is recommended during vertical data invalid period. (refer to the following figure)
In 400 and 350 lines modes, the display position won't be centered on the screen if the vertical sync. signal, TV, doesn't have above typical values.



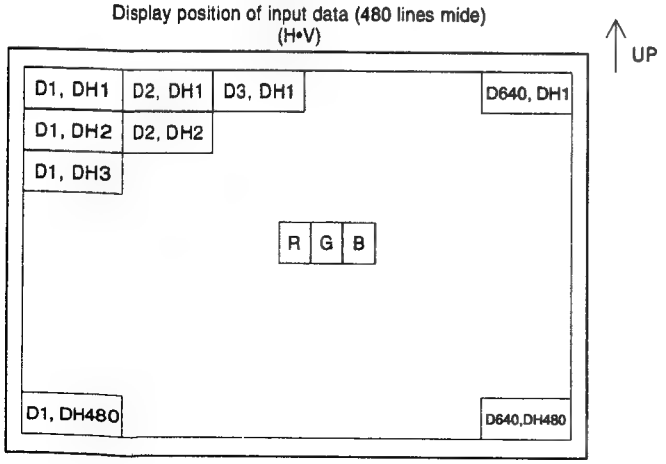
400 lines mode (TV-449)



350 lines mode (TV-449)

6-3. Input Data Signals and Display Position on the screen

Display position of input data (480 lines mide)
(H•V)



6-4. Input Signals, Basic Display Colors and Gray Scale of Each Color

	color & Gray scale	Data signal								
		R0	R1	R2	G0	G1	G2	B0	B1	B2
Basic color	Black	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	1	1	1
	Green	0	0	0	1	1	1	0	0	0
	Light blue	0	0	0	1	1	1	1	1	1
	Red	1	1	1	0	0	0	0	0	0
	Purple	1	1	1	0	0	0	1	1	1
	Yellow	1	1	1	1	1	1	0	0	0
	White	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0
	⇑	1	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0
	⇑	1	1	0	0	0	0	0	0	0
	⇓	0	0	1	0	0	0	0	0	0
	Brighter	1	0	1	0	0	0	0	0	0
	⇓	0	1	1	0	0	0	0	0	0
	Red	1	1	1	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0
	⇑	0	0	0	1	0	0	0	0	0
	Darker	0	0	0	0	1	0	0	0	0
	⇑	0	0	0	1	1	0	0	0	0
	⇓	0	0	0	0	0	1	0	0	0
	Brighter	0	0	0	1	0	1	0	0	0
	⇓	0	0	0	0	1	1	0	0	0
	Green	0	0	0	1	1	1	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0
	⇑	0	0	0	0	0	0	1	0	0
	Darker	0	0	0	0	0	0	0	1	0
	⇑	0	0	0	0	0	0	1	1	0
	⇓	0	0	0	0	0	0	0	0	1
	Brighter	0	0	0	0	0	0	1	0	1
	⇓	0	0	0	0	0	0	0	1	1
	Blue	0	0	0	0	0	0	1	1	1

0: Low level voltage
1: High Level voltage

Each color is displayed in 8 gray scales from 3 bit data signals input. According to the combination of total 9 bit data, 512 colors are displayed.

14. Inverter PWB

1. Application:

This inverter is used for CCFT lamps.

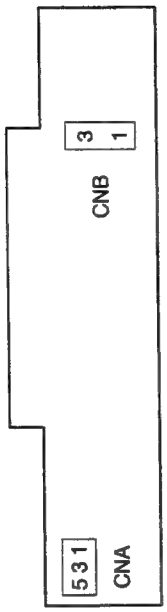
2. Connector pin assignment:

Input : CNA
Model No. : DF3-5P-2H
Supplier : HRS

PIN	SYMBOL
1	Vin
2	Vin
3	Gnd
4	Gnd
5	Cont

Output : CNB
Model No. : SM02 (8.0) B-BHS-1-TB
Supplier : JST

PIN	SYMBOL
1	HV Output
2	N.C.
3	HV Gnd



15. AC Adaptor

1. Scope

This specification defines the performance characteristics of a grounded, single phase, 28 watt, 1 output power supply. This specification also defines worldwide safety and electromagnetic compatibility requirements for the power supply which is intended for use in Note Book products.

2. Input requirements

2.1 Input voltage

	MINIMUM		MAXIMUM		NOMINAL	
LOW RANGE	90	VAC	264	VAC	115/230	VAC

2.2 Frequency

	MINIMUM		MAXIMUM		NOMINAL	
SINGLE PHASE	47	Hz	63	Hz	50/60	Hz

2.3 Voltage selection

A full range will be provided to select the appropriate range.

2.4 Input current

0.7 Amps maximum at 115 VAC input voltage, 0.4 Amps maximum at 230 VAC input voltage and full load condition.

2.5 Inrush current

50 Amps peak maximum for one half cycle of AC (cold start) at any input voltage as specified in paragraph 2.1.

2.6 Power supply efficiency

The power supply efficiency shall not be less than 70 % at nominal continuous input line and full rated output power (At constant voltage mode)

3. Output requirements

3.1 Static dc load

OUTPUT NO.	NOMINAL VOLTAGE (V)	LOAD CURRENT (A)		REGULATION
		MIN.	MAX.	(V)
1	+21.0	0	1.35	±1.0

Note 1: Regulation is the percent of absolute value of nominal output voltage.

3.2 Charging current output

1.35A constant current when system turn off (c.c mode) and 20-40 mA trickle current when system turn on (c.v mode).

3.3 Ripple and noise

The ripple and noise of the outputs shall be measured at the load end of the output cables when terminate to a load impedance as specified in paragraph 3.3.1.

Output Voltage		Ripple & Noise (p-p)	
+21.0	V	180/200	mV

Note 1: 200mV P-P for frequency 20 KHZ to 500 KHZ.
2: 200mV P-P for frequency below 1 KHZ.
3: 180mV P-P noise and spike at 500 KHZ to 20 MHZ.

3.3.1 Load impedance

Filter capacitors are connected to each output. Capacitance values and material type are listed below.

OUTPUT	VOLTAGE NOM.(V)	CAPACITANCE NOM. (μF)	MATERIAL TYPE
1	+21.0	47μF/0.1μF	ELECTROLY./MONO.

3.4 Power noise

The power supply should work normally when AC input voltage appear power noise.

Note: power noise condition:

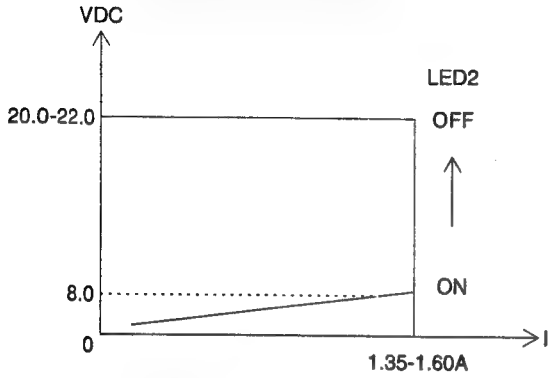
1. Height of impulse 500v.
2. Width of impulse 100ns and 400ns.
3. Synchronous with power supply frequency (0,90 degrees) and asynchronous 55Hz.

3.5 Charging method

Fast charging — Constant current 1.35-1.60 amp charging.

Trickle charging — Constant current 20-40mA when battery is full. (By system control)

Charging voltage — In constant current mode, battery can be fast charged from the survival voltage 8.0VDC min until the voltage reached 20.0VDC min or to 22.0 VDC max. Upon reaching this voltage, LED2 will turn off and the battery be changed to trickle charge mode by system control.



Indicator

Power on – LED1 Green ON
No charging – LED2 off
In charging – LED2 Orange ON
Charge full – LED2 off
Protection – LED1 & LED2 flash (OCP)
– LED1 & LED 2 off (SCP)
– LED 1 ON Only (OVP)

3.6 Hold up time

The power supply unit shall maintain the output voltages within voltage specifications for 1/2 cycle after lost of input power under the condition of nominal input voltage, 50/60Hz frequency maximum output load.

4. Overshoot/under shoot

Any overshoot at turn on or turn off shall be less than ±10% of the nominal output voltage.

5. No load operation

The power supply shall be able to operate under no load condition. No damage to the power supply is allowed and internal component can not be stressed beyond its rating.

6. Frequency of operation

To keep audible noise to a minimum, power supply shall be switched at frequency higher than 20 KHz.

7. Temperature coefficient

The temperature coefficient of all outputs are ±0.03% per degree centigrade maximum.

8. Protection

8.1 Over voltage protection

The power supply should be clamped for any cause of over voltage condition before any output exceeds its limits below.

OUTPUT NO.	NOMINAL OUTPUT VOLTAGE (V)	OVER VOLTAGE	
		MIN.(V)	MAX.(V)
1	+21.0	24	30

The power supply will recover automatically after removal of over voltage condition. Power on reset is not required.

8.2 Short circuit protection

A short circuit placed on any DC output shall cause no damage to and latched off the power supply. The power supply will recover automatically after removal of the short circuit fault. Power on reset is not required.

8.3 Over current protection

The power supply shall provide over current protection. The current limit set point is 1.60A max of full load of the power supply.
The power supply will recover automatically after the overload is removed. Power on reset is not required.

8.4 Lightning surge protection

COMMON MODE: 2KV, 1.2*50μS (LINE, NEUTRAL TO FG)
NORMAL MODE: 2KV, 1.2*50μS (LINE TO NEUTRAL)

9. Power on delay time:

All output voltages shall be within regulation in less than 1 SEC under any input voltage operation range.

10. Safety requirements

The power supply must comply with the following national standards:

- United States Standard: UL:UL1950
- Canadian Standard: CSA:CSA C22.2 No.234
- European Standards: TUV: EN 60 950
- Nordic Countries Standard: NEMKO:NEK-EN 60 950 + EN 60 950/A1/A2

10.1 Dielectric withstand

Primary to Secondary: 1800 Var, 3 sec.
1500 Var, 1 min.

10.2 Insulation resistance

Primary to Secondary: 20 Meg. ohms Min., 500VDC

10.3 Ground leakage current

The power supply ground leakage shall be less than 0.75 mA.

11. Electromagnetic compatibility

Emissions Radiated/Conducted Spec.:
–6db below all applicable standards listed below.
(standard -6db margin)

Emissions FCC:
Class B Part 15 Sections 15.830 and section 15.832.

Emissions CISPR:
C.I.S.P.R. Publication NO.22,ECMA95(March 1985).

Emissions VDE:
EC STD (IEC801-3)

Compliance Test Procedure.
Agency approval will be done per specification standard.
(ie 3 meter for FCC, 10 meter for VDE etc.)

12. Environment

12.1 Operating

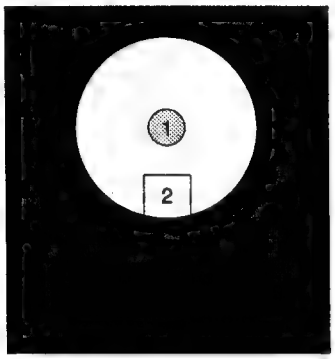
Temperature: 4 to 38 degrees centigrade
Relative Humidity: 10 to 90 percent, non-condensing

12.2 Shipping and storage

Temperature: –40 to 85 degrees centigrade
Relative Humidity: 10 to 90 percent, non-condensing

Connectors

Adaptor CON (JP3)



Pin	Signal
1	DC_IN (21V)
2	GND

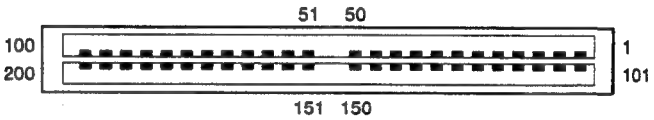
16. Nickel-Metal Battery

15-1 Specifications

Type	Rechargeable Nickel-Metal hydride
Weight	1.063 pounds (0.54kg)
Nominal Capacity	1800mA
Nominal Voltage	14.4V
Standard Charge current	230mA
Temperature (recommended)	
Charge	0°C to 45°C
Discharge	–20° to 60°C
Storage	–30° to 50°C
Storage (Long Period)	–30° to 35°C

17. Expansion Connectors

200 pin expansion Connector (CON6)



Pin	Signal
1	VESA - D0
2	VESA - D1
3	VESA - D2
4	VESA - D3
5	VESA - D4
6	VESA - D5
7	VESA - D6
8	VESA - D7
9	VESA - D8
10	GND
11	VESA - D9
12	VESA - D10
13	VESA - D11
14	VESA - D12
15	VESA - D13
16	VESA - D14
17	VESA - D15
18	VESA - D16
19	VESA - D17
20	GND
21	VESA - D18
22	VESA - D19
23	VESA - D20
24	VESA - D21
25	VESA - D22
26	VESA - D23
27	VESA - D24
28	VESA - D25

Pin	Signal
29	VESA - D26
30	GND
31	VESA - D27
32	VESA - D28
33	VESA - D29
34	VESA - D30
35	VESA - D31
36	GND
37	ISA - RESET
38	ISA - IOCHRDY
39	ISA - TC
40	ISA - BALE
41	ISA - SBHE*
42	ISA - AEN
43	ISA - SMEMR*
44	ISA - SMEMW*
45	ISA - IOR*
46	ISA - IOW*
47	ISA - MEMR*
48	ISA - MEMW*
49	DOCKING INSTALLED*
50	DOCKING POWER ON
51	VESA - BE0*
52	VESA - BE1*
53	VESA - BE2*
54	VESA - BE3*
55	VESA - A2
56	VESA - A3

Pin	Signal
57	VESA - A4
58	VESA - A5
59	VESA - A6
60	GND
61	VESA - A7
62	VESA - A8
63	VESA - A9
64	VESA - A10
65	VESA - A11
66	VESA - A12
67	VESA - A13
68	VESA - A14
69	VESA - A15
70	GND
71	VESA - A16
72	VESA - A17
73	VESA - A18
74	VESA - A19
75	VESA - A20
76	VESA - A21
77	VESA - A22
78	VESA - A23
79	VESA - A24
80	GND
81	VESA - A25
82	VESA - A26
83	VESA - A27
84	VESA - A28

Pin	Signal
85	VESA - A29
86	VESA - A30
87	VESA - A31
88	VESA - VLBICS*
89	VESA - RDY*
90	GND
91	VESA - CPUCLK
92	GND
93	VESA - D/C*
94	VESA - W/R*
95	VESA - M/IO*
96	VESA - ADS*
97	VESA - BRDY*
98	VESA - BLAST*
99	VESA - RESET*
100	IO-SLICE INSTALLED*
101	DOCKING POWER
102	DOCKING POWER
103	DOCKING POWER
104	DOCKING POWER
105	ISA - SD0
106	ISA - SD1
107	ISA - SD2
108	ISA - SD3
109	ISA - SD4
110	ISA - SD5
111	ISA - SD6
112	ISA - SD7

Pin	Signal
113	ISA - SD8
114	ISA - SD9
115	GND
116	ISA - SD10
117	ISA - SD11
118	ISA - SD12
119	ISA - SD13
120	ISA - SD14
121	ISA - SD15
122	VCC (5V)
123	VCC (5V)
124	VCC (5V)
125	VCC (5V)
126	ISA - IRQ3
127	GND
128	ISA - IRQ4
129	ISA - IRQ5
130	ISA - IRQ7
131	BATTERY CHARGE IN
132	BATTERY CHARGE IN
133	BATTERY CHARGE IN
134	BATTERY CHARGE IN

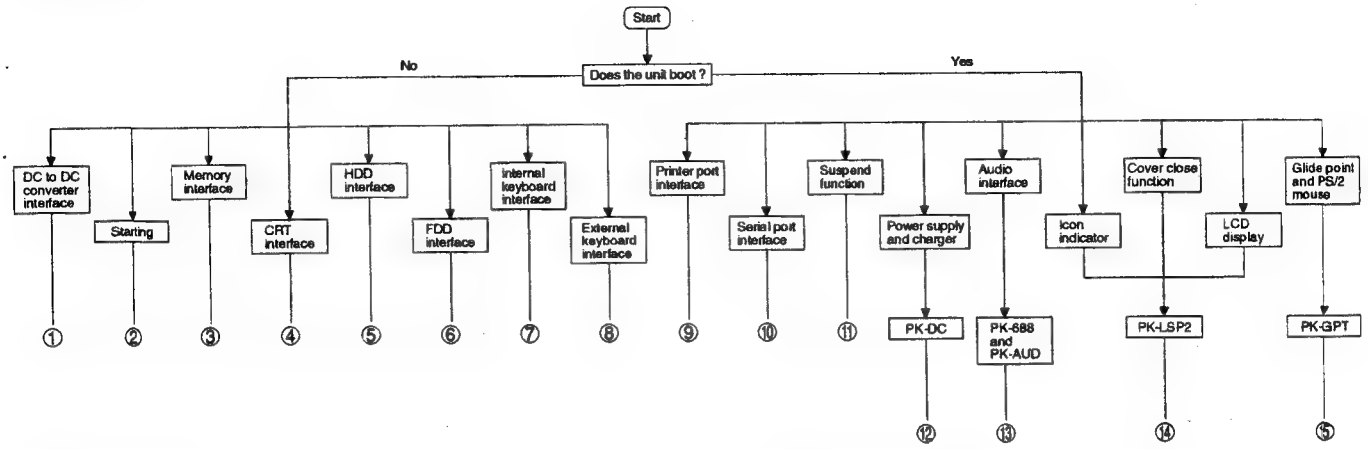
Pin	Signal
135	ISA - IRQ9
136	ISA - IRQ10
137	ISA - IRQ11
138	GND
139	ISA - IRQ15
140	ISA - MEMCS16*
141	ISA - IOCS16*
142	ISA - OWS*
143	ISA - REF*
144	ISA - IOCHCK*
145	ISA - MASTER*
146	GND
147	PS2 - MSCLK
148	PS2 - MSDATA
149	PS2 - KBDATA
150	PS2 - KBCLK
151	ISA - SA0
152	ISA - SA1
153	ISA - SA2
154	ISA - SA3
155	ISA - SA4
156	ISA - SA5

Pin	Signal
157	ISA - SA6
158	ISA - SA7
159	ISA - SA8
160	GND
161	ISA - SA9
162	ISA - SA10
163	ISA - SA11
164	ISA - SA12
165	ISA - SA13
166	ISA - SA14
167	ISA - SA15
168	ISA - SA16
169	ISA - SA17
170	ISA - SA18
171	ISA - SA19
172	GND
173	ISA - SA20
174	ISA - SA21
175	ISA - SA22
176	ISA - SA23
177	ISA - SYSCLK
178	ISA - DRQ0

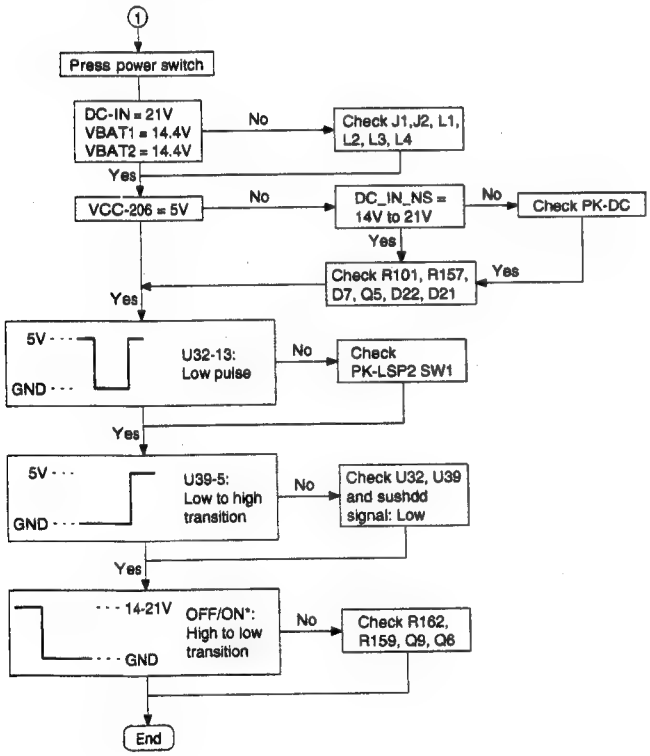
Pin	Signal
179	ISA - DRQ1
180	ISA - DRQ3
181	ISA - DRQ5
182	ISA - DRQ6
183	ISA - DRQ7
184	GND
185	ISA - DACK0*
186	ISA - DACK1*
187	ISA - DACK3*
188	ISA - DACK5*
189	ISA - DACK6*
190	ISA - DACK7*
191	MIDI IN
192	GND
193	MIDI OUT
194	SPEAKER LEFT
195	SPEAKER RIGHT
196	VGA - RED
197	VGA - GREEN
198	VGA - BLUE
199	VGA - VSYNC
200	VGA - HSYNC

CHAPTER 5. TRAUBLE SHOOTING

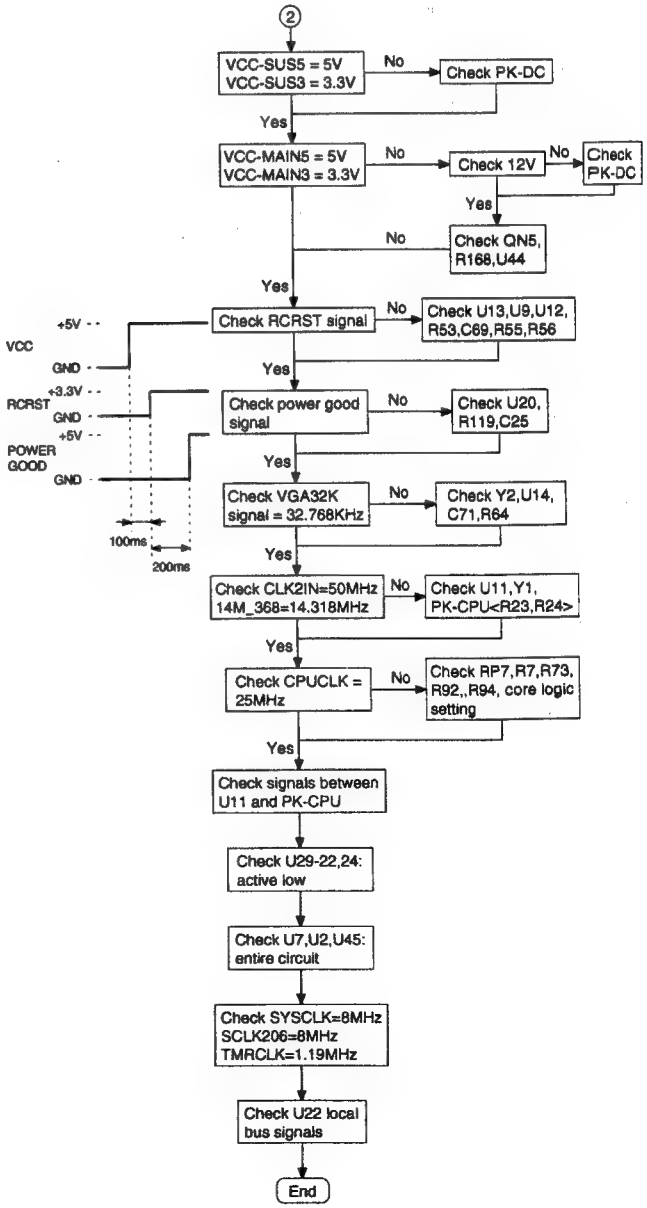
1. General



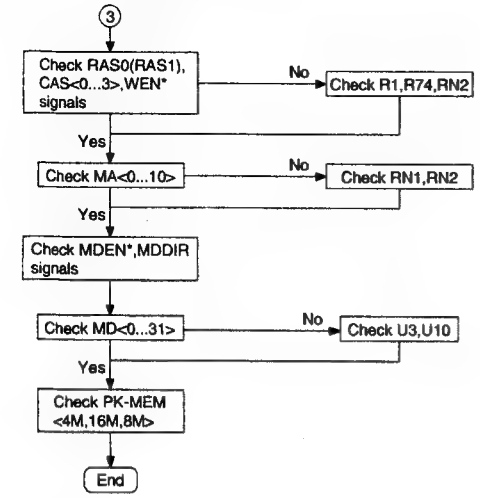
1-1. DC-DC converter interface



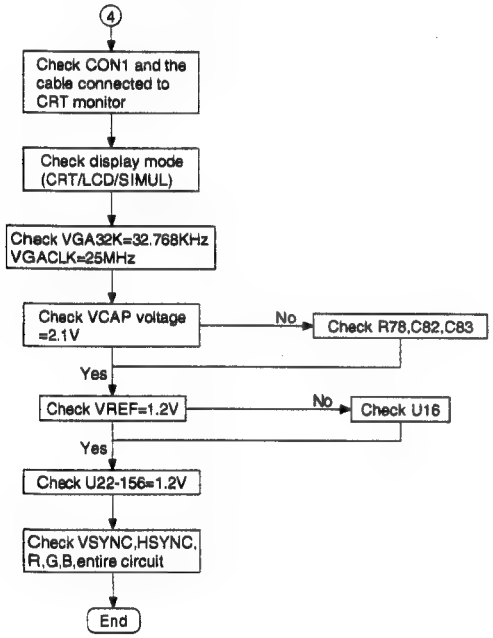
1-2. Starting check



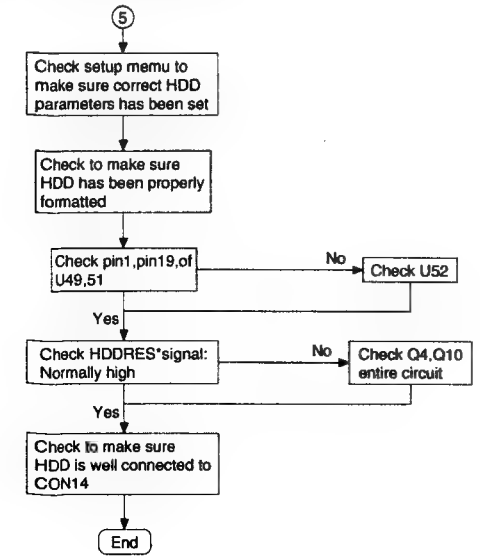
1-3. Memory interface check



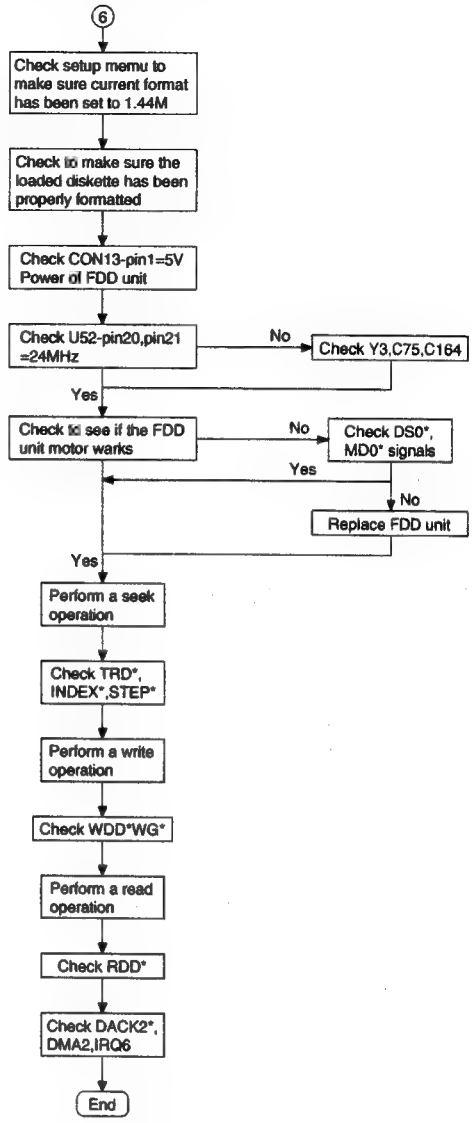
1-4. CRT interface check



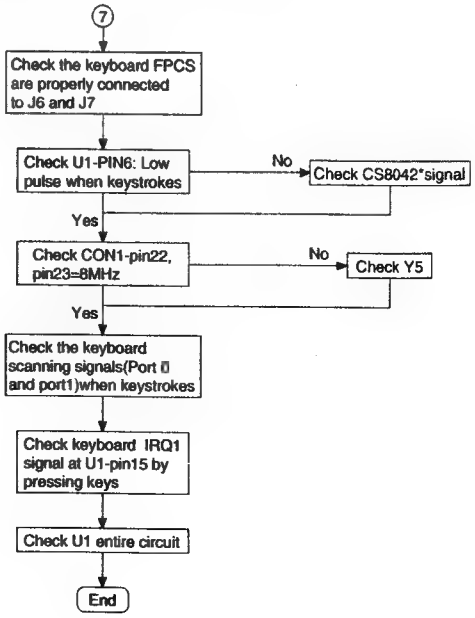
1-5. HDD interface check



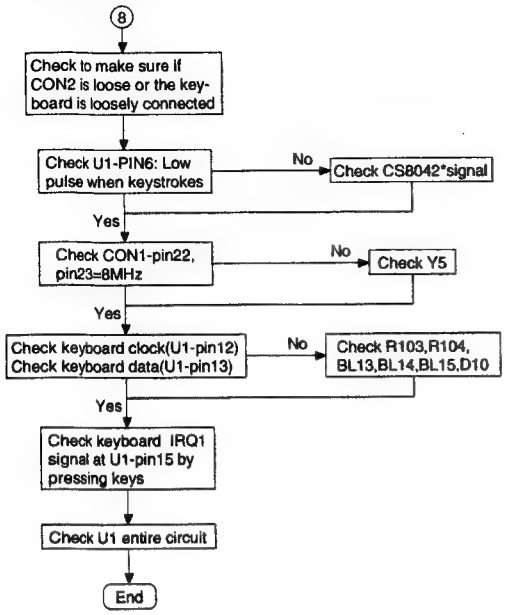
1-6. FDD interface check



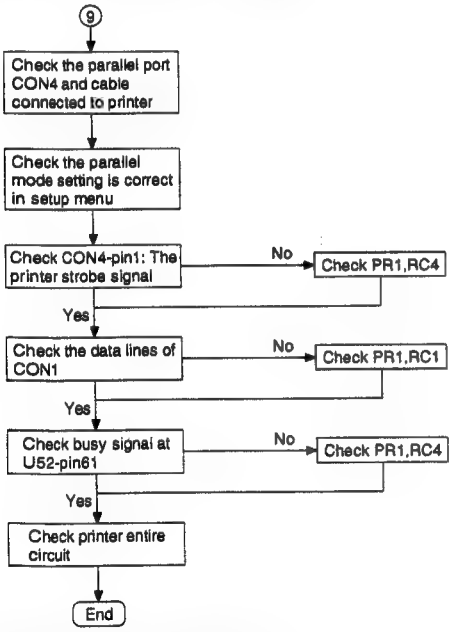
1-7. Internal keyboard check



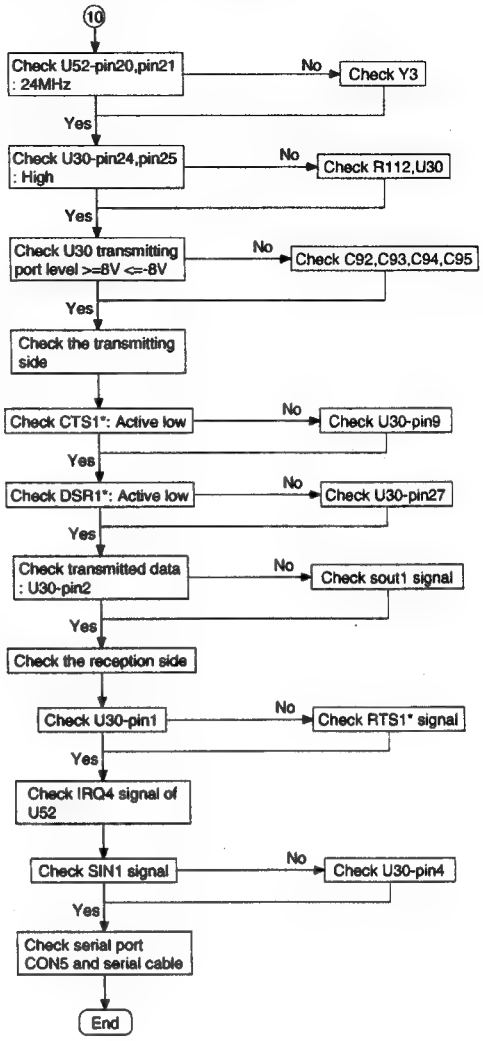
1-8. External keyboard check



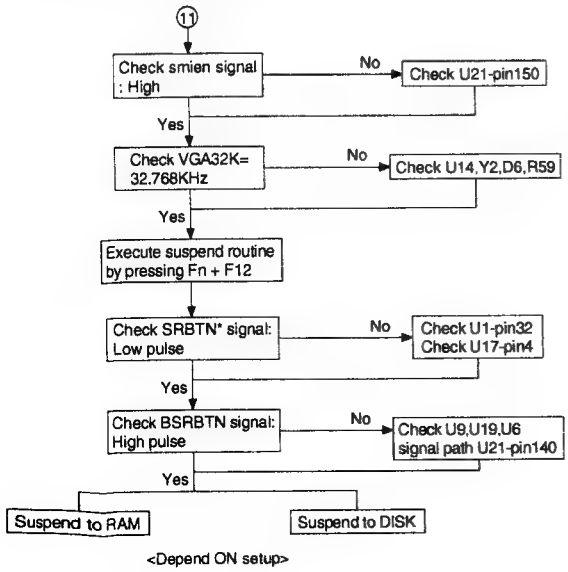
1-9. Printer port interface check

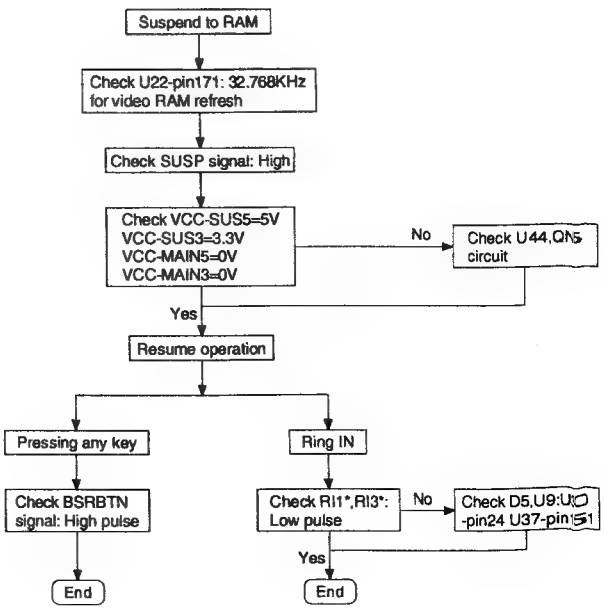


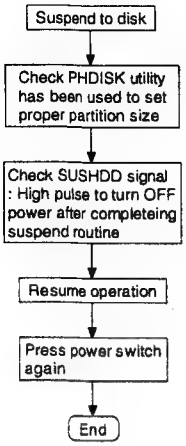
1-10. Serial port interface check



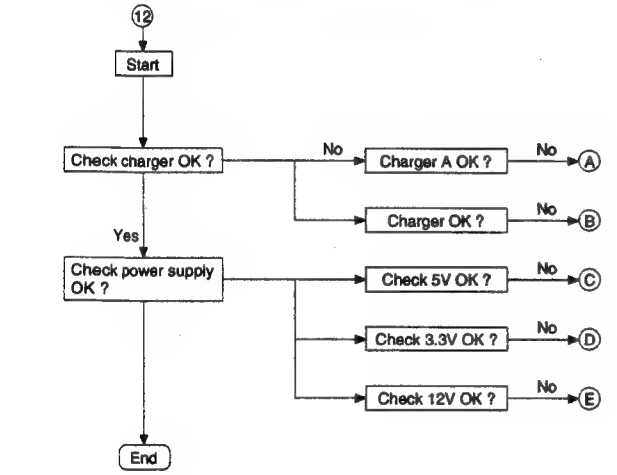
1-11. Suspend function check

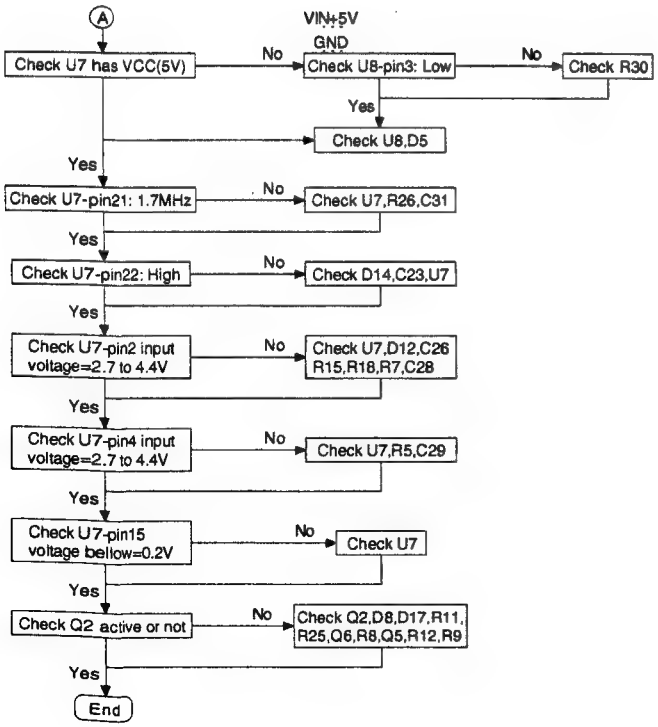


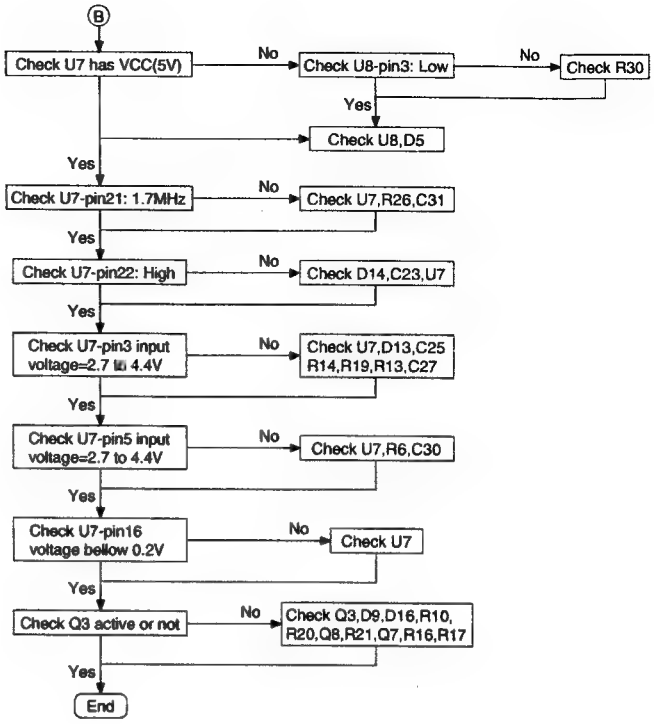


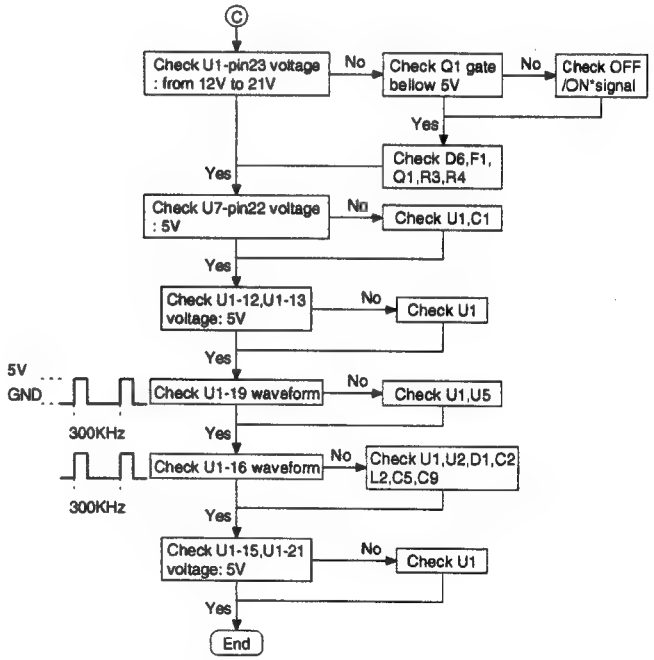


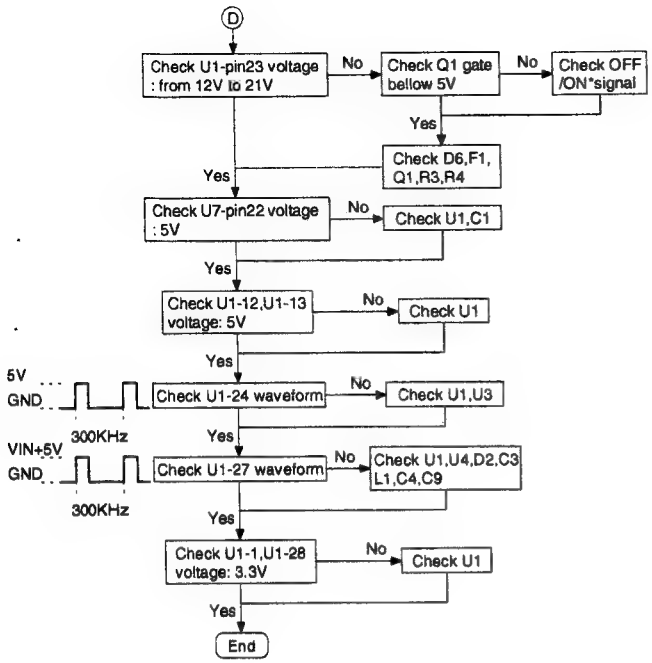
1-12. Power supply and charging check (PK-DC)

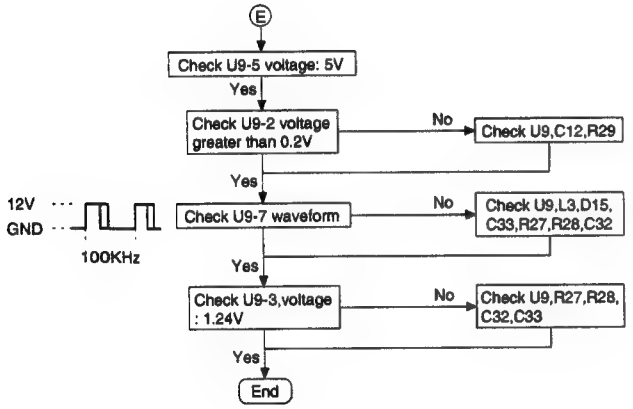




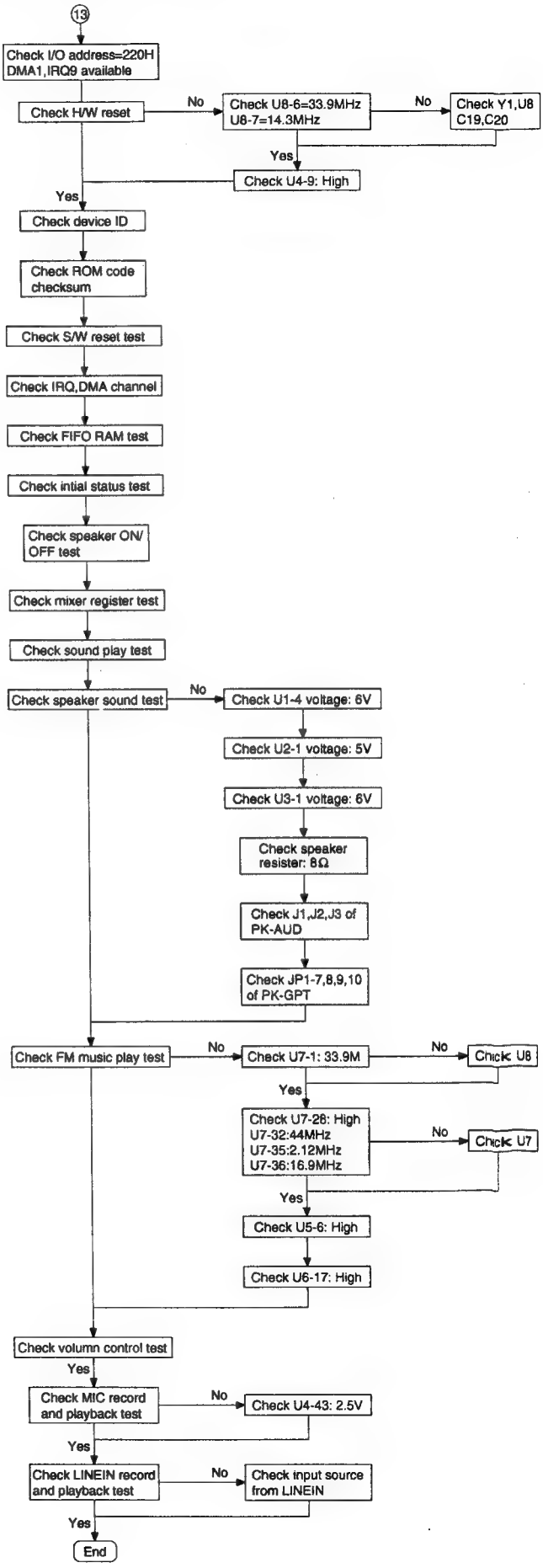




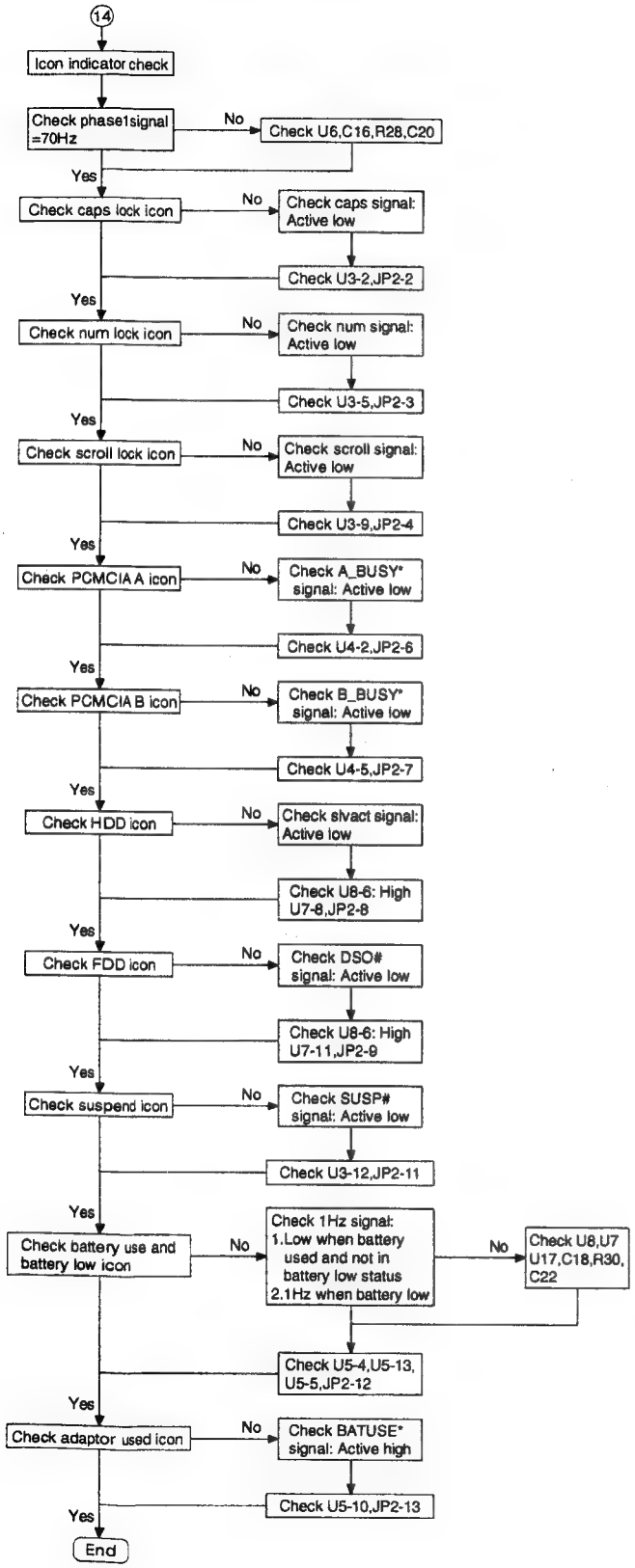


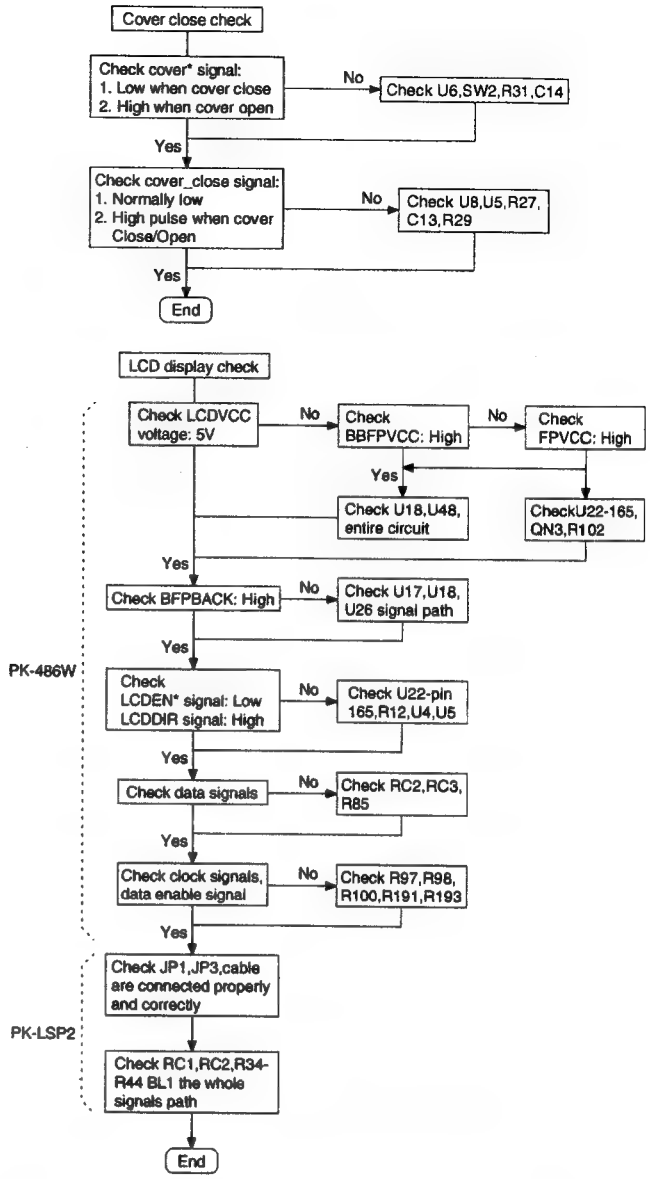


1-13. Audio check (PK-688)

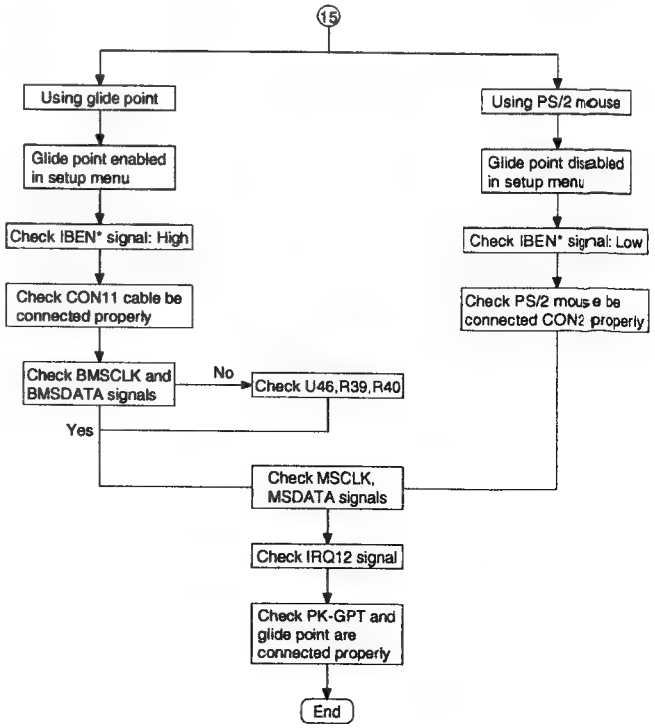


1-14. Icon indicator, cover close function LCD display check (PK-LSP2)





1-15. Glide point and PS/2 mouse interface check



CHAPTER 6. DIAGNOSTIC PROGRAM

The diagnostic program tests the proper functioning of the system. If the Power On Self Test routine doesn't display any messages, but you suspect that there is a problem, run the diagnostic program that has the following items:

- Real Time CLock
- Memory
- Keyboard
- Video Subsystem
- Liquid Crystal Display
- Floppy Disk Drive
- Printer
- Hard Disk Drive
- Setup Utility
- PCMCIA
- IR Port
- Audio

1. Creating a Diagnostic Program Diskette

The diagnostic programs are stored in the SHPUTY directory on the support diskette number 1 and also in the SHPUTY directory on your hard disk drive. The diagnostics programs are:
DIAG.EXE, SC_LOWT.EXE, SC_UPT.EXE, SC_IRT.EXE and SC_AUD.EXE.

Create a diagnostics diskette as follows:

1. Insert a new diskette into the floppy disk drive and format it using the following command:

`c:\>FORMAT A:/S` **Enter**

(or `FORMAT A: /S /F:720` in the case of a 2DD diskette)

Setup Utility
This item accesses the Setup utility. However, if you make changes in the Setup utility, the system will reboot and you cannot return to the diagnostic program.

PCMCIA
Checks the interrupt of the card status change.

IR Port
Checks the IR port Loop Back Test.

Audio
This item includes the following tests:
Reset test
IRQ test
DMA test
FIFO RAM test
Speaker test
Microphone test checks recording and playing.

2. Then type:

`COPY \SHPUTY\DIAG.EXE A:` **Enter**

Repeat the command for the files SC_LOWT.EXE, SC_UPT.EXE, SC_IRT.EXE and SC_AUD.EXE.
You have now created a diagnostic program diskette.

2. Starting the Diagnostic Program

The diagnostic program should always be run from the floppy disk drive:

1. Change the Boot From item in Setup utility to FDD.
2. Insert the diagnostic program diskette you created in the previous section into the floppy disk drive, boot up the system, then at the A:\>prompt, type:

   `A:\>DIAG` **Enter**

   The diagnostic program starts up. After several seconds, the main menu will be displayed on the screen.
3. Use the arrow keys to move the bar cursor to the particular diagnostic test you want to run and press **Enter**. Or, press **Esc** to exit the diagnostic program and return to the A:\>prompt.

Some of the diagnostic test categories on the menu contain several separate tests. When you select one of these categories, a separate submenu is displayed. You can exit the submenu and return to the main menu by pressing **Esc**. Each category is described below.

After finishing the diagnostics program, you should restart your computer by pressing **Ctrl + Alt + Del** then change the Boot From item in the Setup utility back to HDD.

Caution: Do not touch the GlidePoint while you are checking your system with the diagnostic program.

Real Time Clock (RTC)

This test contains the following three tests:

FTC timer check

Checks if the timer interrupt works correctly.

RTC clock check

Checks if the clock works correctly.

CMOS RAM check

Does a data read/write check on the special battery back up memory area used for the realtime clock.

Run all checks

Runs all three of the checks above in sequence.

Memory

This test contains the following checks:

Caution: These checks will destroy the contents of the memory.

Conventional memory check

Reads/writes data in the conventional memory area. The check stops at the first error and displays an error message.

Extended memory check

Reads/writes data in the extended memory area. The check stops at the first error and displays an error message.

Run all checks

Runs the two checks above in sequence.

Keyboard

After selecting this test, you are prompted for the keyboard type. Move the bar cursor using the arrow keys to select either the U.S. English keyboard or other keyboard types and press **Enter**.
The keyboard test begins with a graphic representation of the keyboard layout displayed on the screen. To test whether a particular key functions properly, press the key. A square should display on the keyboard layout at that position if the key is working correctly.

Video Subsystem

This test checks that the built-in video subsystem is working properly. The video subsystem menu is displayed on the screen with the following categories:

Video memory check

Checks the buffer in the video subsystem.

DAC check

Checks the digital-to analog converter in the VGA subsystem.

Attribute check

Displays 16 foreground, 8 background, and 8 blinking shades of gray.

Character set check

Displays characters on the screen normally on an 80 x 25 text mode display.

Run all checks

Runs all four of the above checks in sequence.

Liquid Crystal Display

This item checks the system's LCD screen. Three test patterns are displayed. A defect in any pattern indicates a faulty screen.

Checker pattern check

A checked pattern is displayed.

Striped pattern check

A striped pattern is displayed.

Shades of color check

64 shades of color are displayed.

Run all checks

Runs all three checks in sequence.

Floppy Disk Drive

This test reads and writes data continuously from/to a diskette in the floppy disk drive to test the read/write functions of the drive. After selecting the test, the floppy drive submenu is displayed with the following categories:

Caution: As the write-read check may erase data from the diskette in the drive under test, use a blank diskette or one containing data that you no longer need.

Read check

Checks that data can be read from the diskette without errors. The test stops if an error is detected and displays an error message.

Write-read check

Checks if data can be written/read correctly by comparing data written to the diskette with data read from the diskette. This test destroys all existing data on the diskette. The test stops if an error is detected and displays an error message.

Printer

This test checks the operation of the printer, if one is connected. After selecting the test, the printer submenu is displayed on the screen with the following categories:

Status check

The printer status signals are checked and displayed.
The following status categories are checked:

Bsy checks the printer busy signal

Ack checks that the printer can handshake with the system

Pe checks that the paper is set

Sel shows when the printer is online

Ioe checks that the printer's mechanical components are functioning properly.

An asterisk is displayed under each category when its check has completed without error.

Print check

Test printing will not start until the five status categories in the status check all show an asterisk (under the category). If a hardware malfunction is detected, an asterisk will not appear below the corresponding category. In this case, you will not be able to do a test print. Make a note of the error message, and contact your Sharp dealer.
Once all categories contain asterisks, press any key. The system returns to the printer submenu. Try the print check. A test pattern should print.

Hard Disk Drive

This test reads and writes data continuously from/to the hard disk to test the read/write functions of the drive. After selecting the test, the hard disk submenu is displayed on the screen.

Caution: DO NOT run the hard disk drive write-read check on the diagnostic program unless you have exhausted all other possibilities, because the test will destroy all existing data on your hard disk.

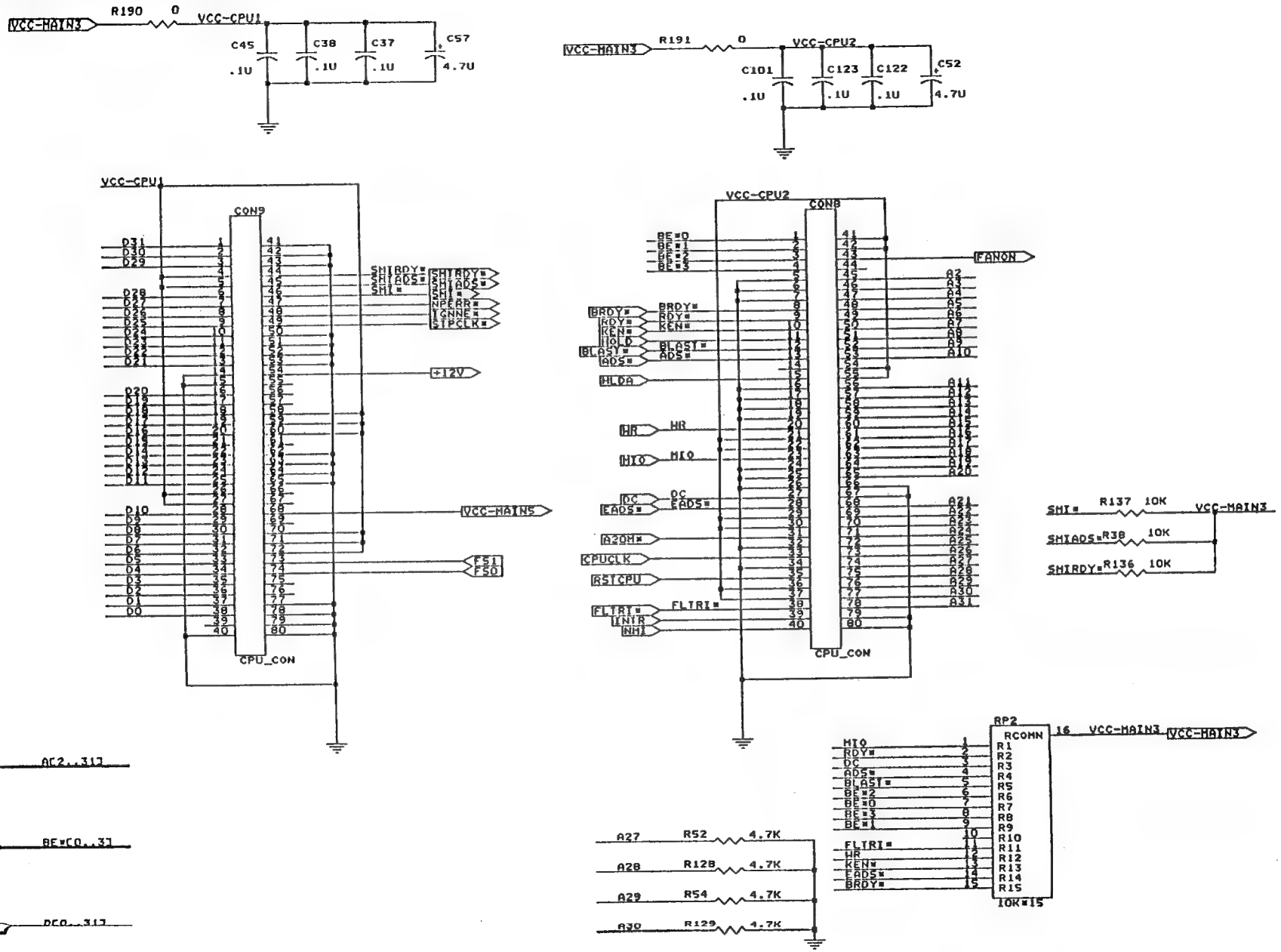
Read check

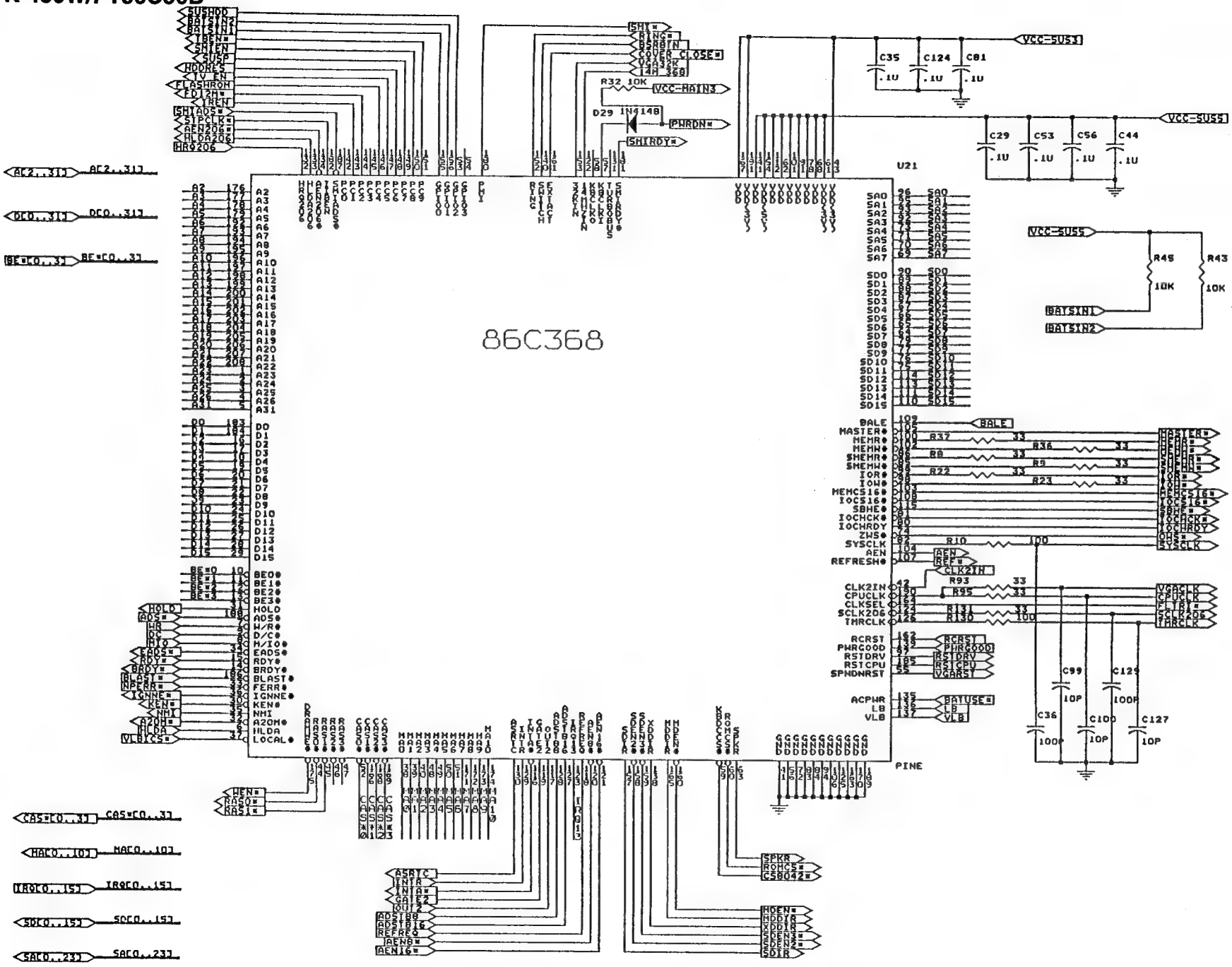
Checks that data can be read from the hard disk without errors. The test stops if an error is detected and displays an error message.

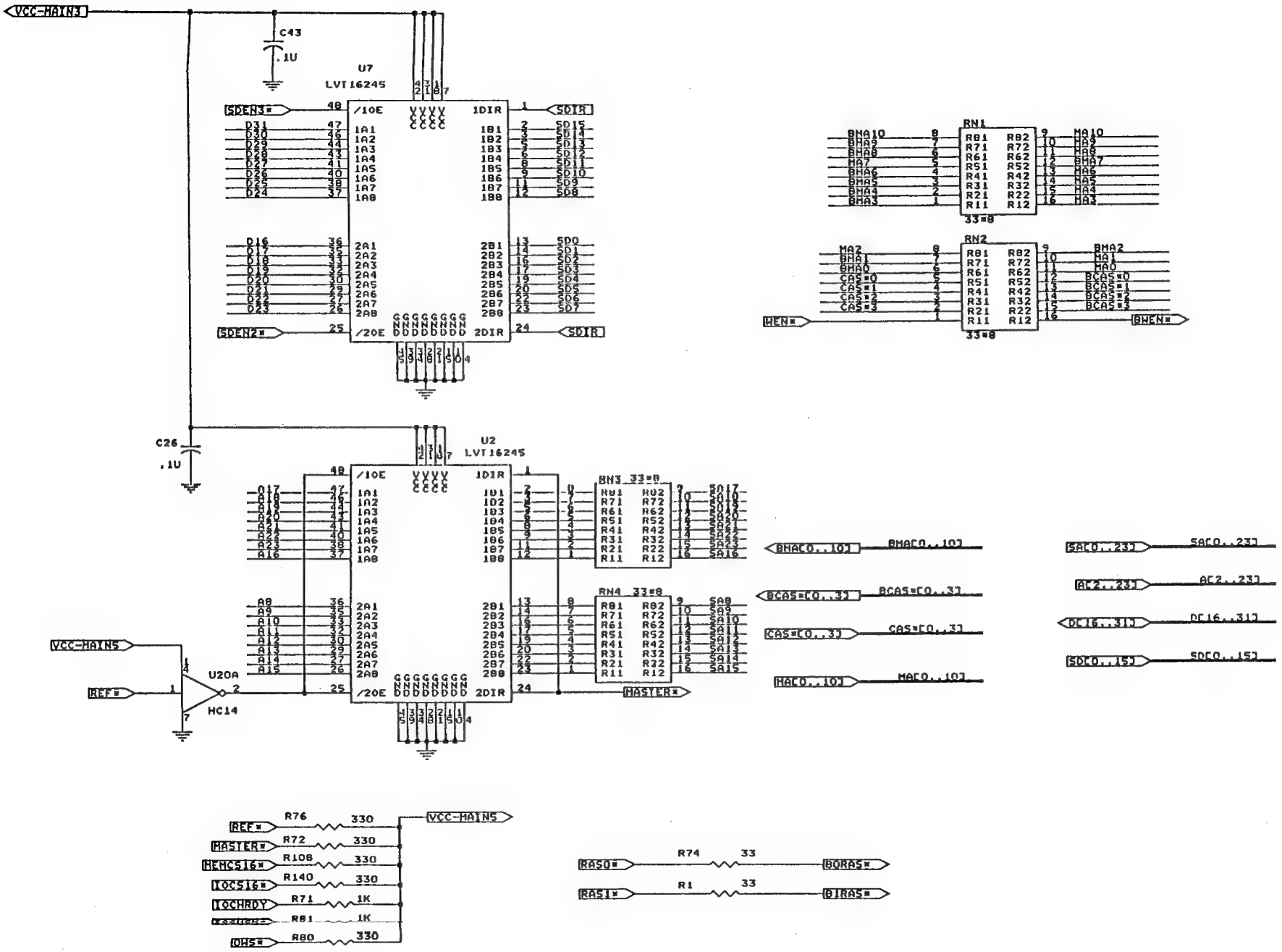
Write-read check

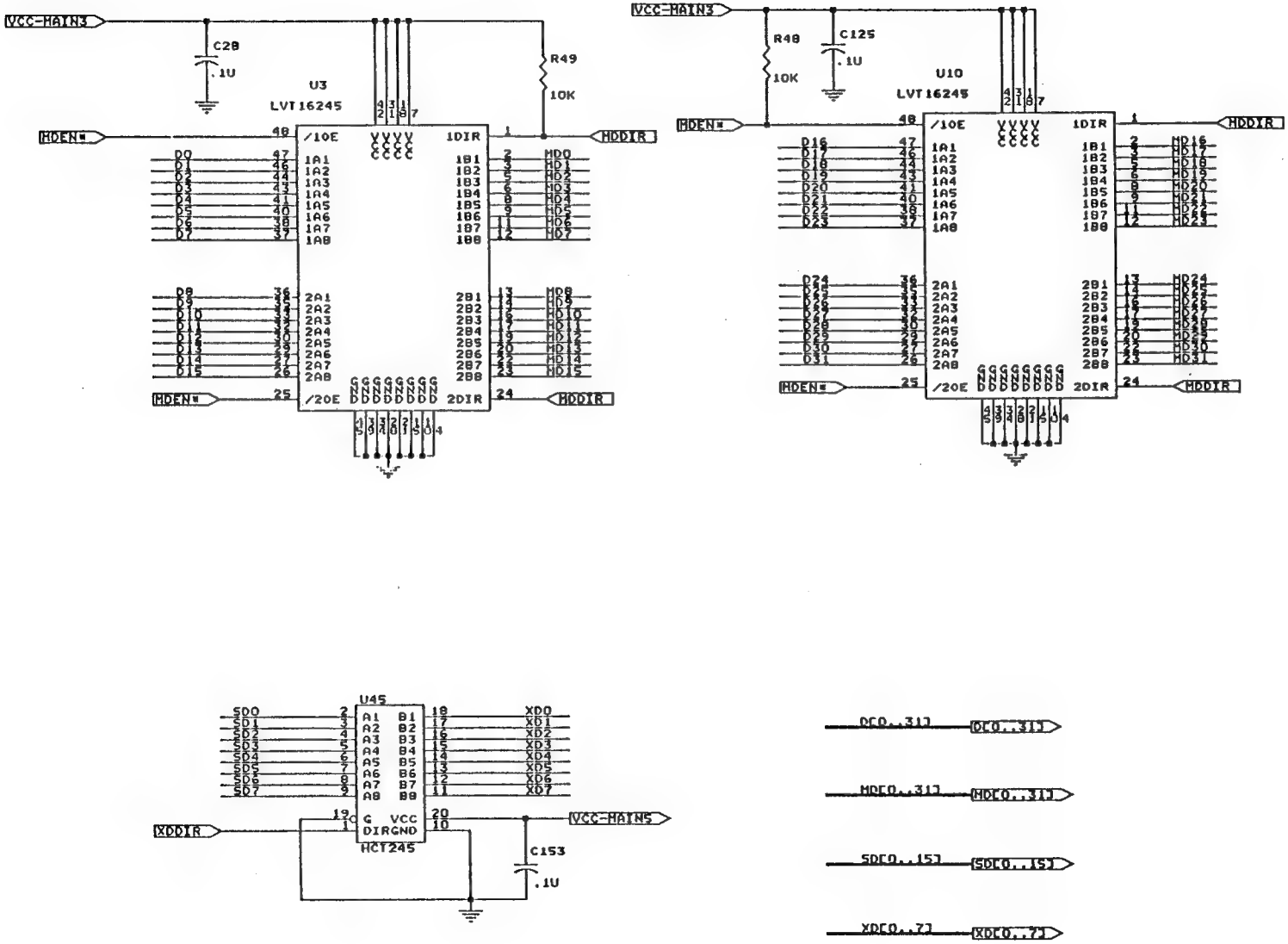
Checks if data can be written/read correctly by comparing data written to the hard disk with data read from the hard disk. This test destroys all existing data on the disk. The test stops if an error is detected and displays an error message. Do not run this test unless you have reason to believe there is a problem with your hard disk.

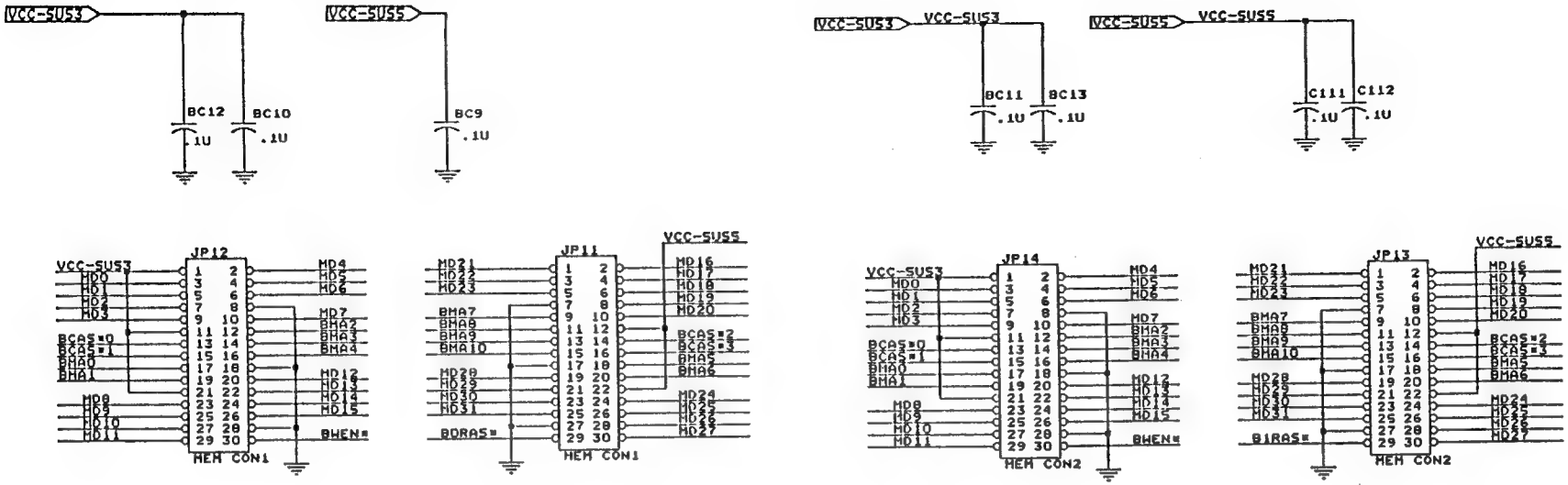
PK-486W/CPU adapter connector

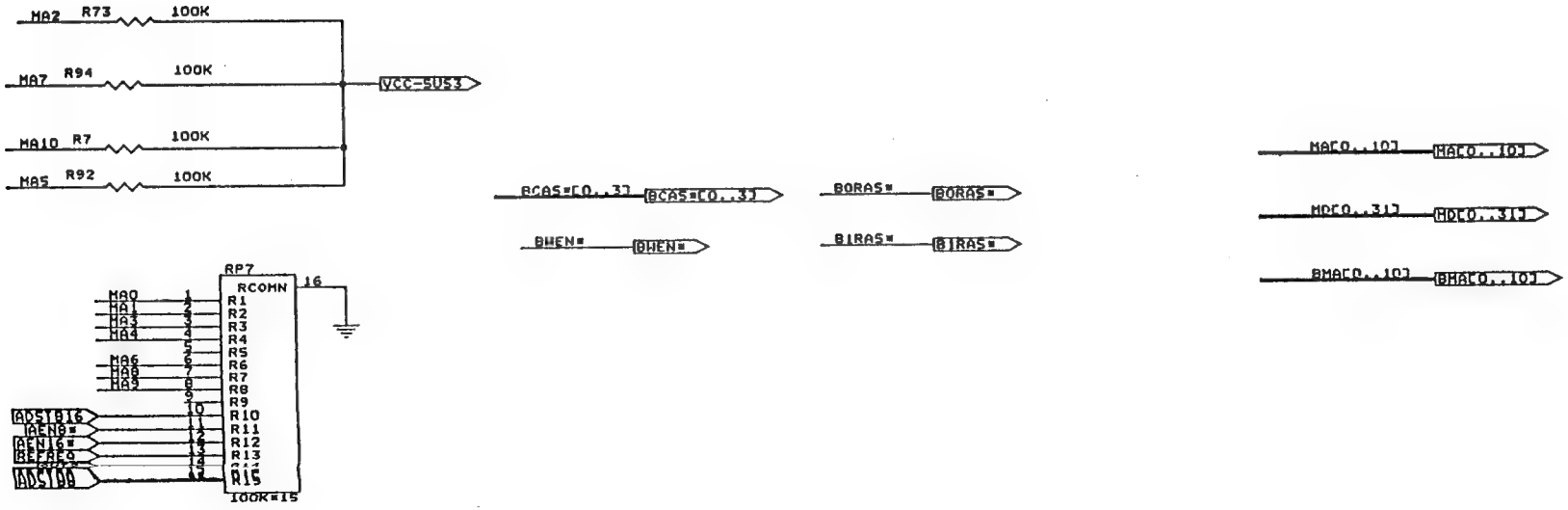


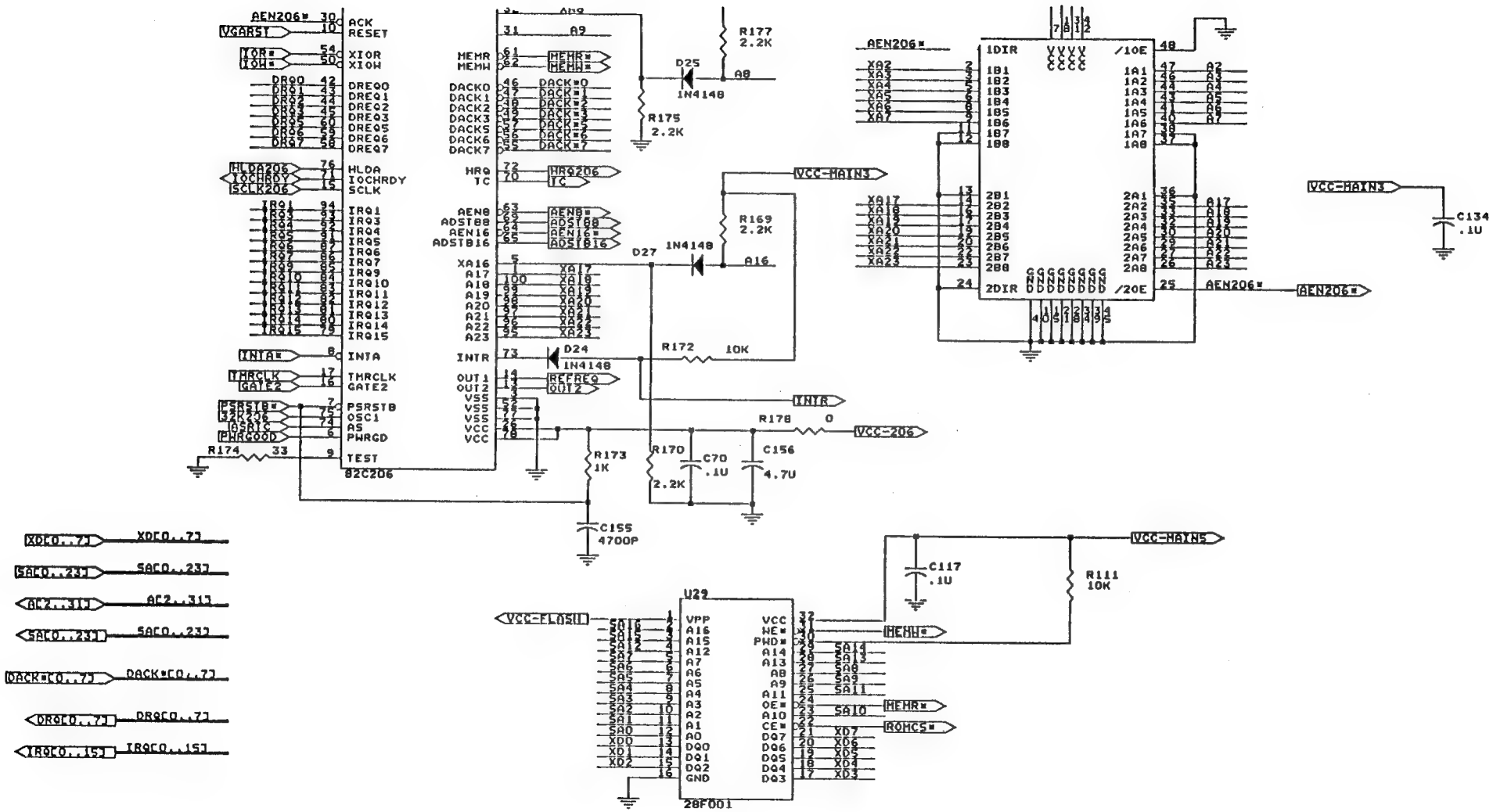

86C368
U21
PINE
VCC-5USB
VCC-MAIN3
PWRDN#
SHIRDY#
D29 1N4148
R32 10K
C35
C124
C81
C29
C53
C56
C44
R45
R43
10K
BATSIN
BATSIN2
BALE
MASTER#
MEMR#
MEMW#
SMEMR#
SMEMW#
IOR#
IOW#
MEMCS16#
IOCS16#
SBHE#
IOCHCK#
IOCHRDY
ZWS#
SYSCLK
AEN
REFRESH#
CLK2IN
CPUCLK
CLKSEL
SCLK206
IHRCLK
RCRST
PWRGOOD
RSTDRV
RSTCPU
SPNDNRST
ACPHR
LB
VLB
BATUSE#
C99
C129
C36
C100
C127
10P
100P
HOLD
ADS#
W/R#
D/C#
M/IO#
EADS#
RDY#
BRDY#
BLAST#
FERR#
IGNNE#
KEN#
NMI
A20M#
HLDA
LOCAL#
VLBUCS#
HEN
NAS0#
RAS1#
SPKR
ROMCS#
CS8042#
HOEN#
MDDIR
XDDIR
SDEN1#
SDEN2#
SDIR
AC2..31
DC0..31
BE#C0..3
CAS#C0..3
HAC0..10
IRQC0..15
SDC0..15
SAC0..23

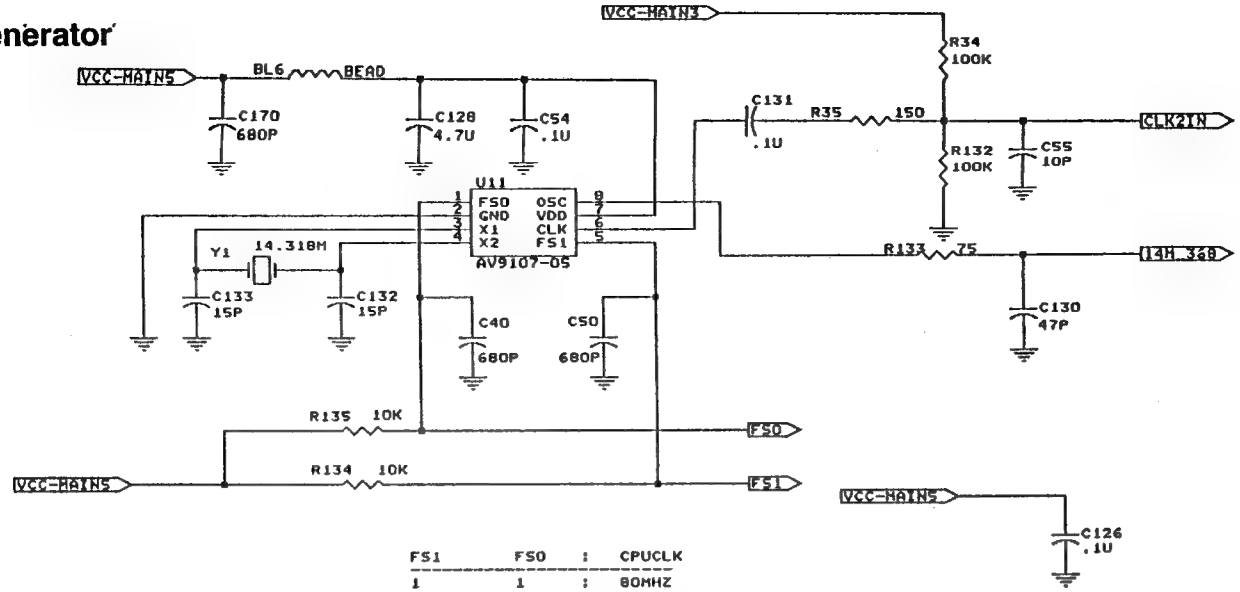

VCC-MAIN3
C43
.1U
U7
LVT16245
SDEN3#
SDEN2#
SDIR
/1OE
/2OE
1DIR
2DIR
C26
.1U
U2
LVT16245
RN1
RN2
RN3 33*8
RN4 33*8
33*8
BMA10
BMA9
BMA8
MA7
BMA6
BMA5
BMA4
BMA3
MA2
BMA1
BMA0
CAS#0
CAS#1
CAS#2
CAS#3
HEN#
BWEN#
BMAC0..10]
BCAS#[0..3]
CAS#[0..3]
MAC0..10]
SAC0..23]
AC2..23]
DC16..31]
SDC0..15]
VCC-MAIN5
REF#
U20A
HC14
MASTER#
R76 330
R72 330
R108 330
R140 330
R71 1K
R81 1K
R80 330
HEMCS16#
IOCS16#
IOCHRDY
OWS#
RAS0#
RAS1#
R74 33
R1 33
B0RAS#
B1RAS#


VCC-MAIN3
C28
.1U
U3
LVT16245
R49
10K
MDEN*
/1OE
1DIR
MDDIR
D0
D1
D2
D3
D4
D5
D6
D7
1A1
1A2
1A3
1A4
1A5
1A6
1A7
1A8
1B1
1B2
1B3
1B4
1B5
1B6
1B7
1B8
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
D8
D9
D10
D11
D12
D13
D14
D15
2A1
2A2
2A3
2A4
2A5
2A6
2A7
2A8
2B1
2B2
2B3
2B4
2B5
2B6
2B7
2B8
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
/2OE
2DIR
R48
10K
C125
.1U
U10
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
MD16
MD17
MD18
MD19
MD20
MD21
MD22
MD23
MD24
MD25
MD26
MD27
MD28
MD29
MD30
MD31
U45
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
G
DIR
VCC
GND
HCT245
XDDIR
VCC-MAIN5
C153
.1U
DC0..31]
MDC0..31]
SDC0..15]
XDC0..7]

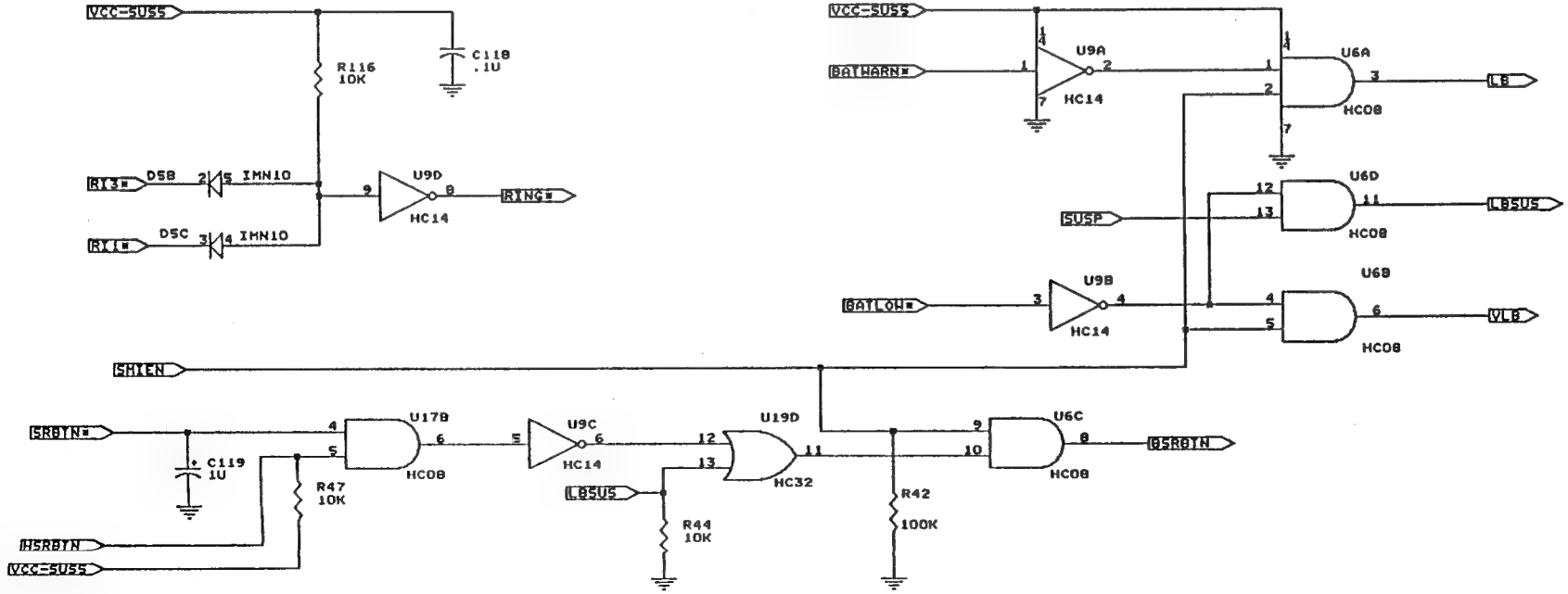

VCC-5VS3
BC12
.1U
BC10
.1U
VCC-5VS5
BC9
.1U
VCC-5VS3
VCC-5VS3
BC11
.1U
BC13
.1U
VCC-5VS5
VCC-5VS5
C111
.1U
C112
.1U
JP12
VCC-5VS3
MD0
MD1
MD2
MD3
MD4
MD5
BCAS#0
BCAS#1
BMA0
BMA1
MD8
MD9
MD10
MD11
MD4
MD5
MD6
MD7
BMA2
BMA3
BMA4
MD12
MD13
MD14
MD15
BWEN#
MEM CON1
JP11
MD21
MD22
MD23
BMA7
BMA8
BMA9
BMA10
MD28
MD29
MD30
MD31
BORAS#
MD16
MD17
MD18
MD19
MD20
BCAS#2
BCAS#3
BMA5
BMA6
MD24
MD25
MD26
MD27
VCC-5VS5
MEM CON1
JP14
VCC-5VS3
MD0
MD1
MD2
MD3
BCAS#0
BCAS#1
BMA0
BMA1
MD8
MD9
MD10
MD11
MD4
MD5
MD6
MD7
BMA2
BMA3
BMA4
MD12
MD13
MD14
MD15
BWEN#
MEM CON2
JP13
MD21
MD22
MD23
BMA7
BMA8
BMA9
BMA10
MD28
MD29
MD30
MD31
B1RAS#
MD16
MD17
MD18
MD19
MD20
BCAS#2
BCAS#3
BMA5
BMA6
MD24
MD25
MD26
MD27
VCC-5VS5
MEM CON2

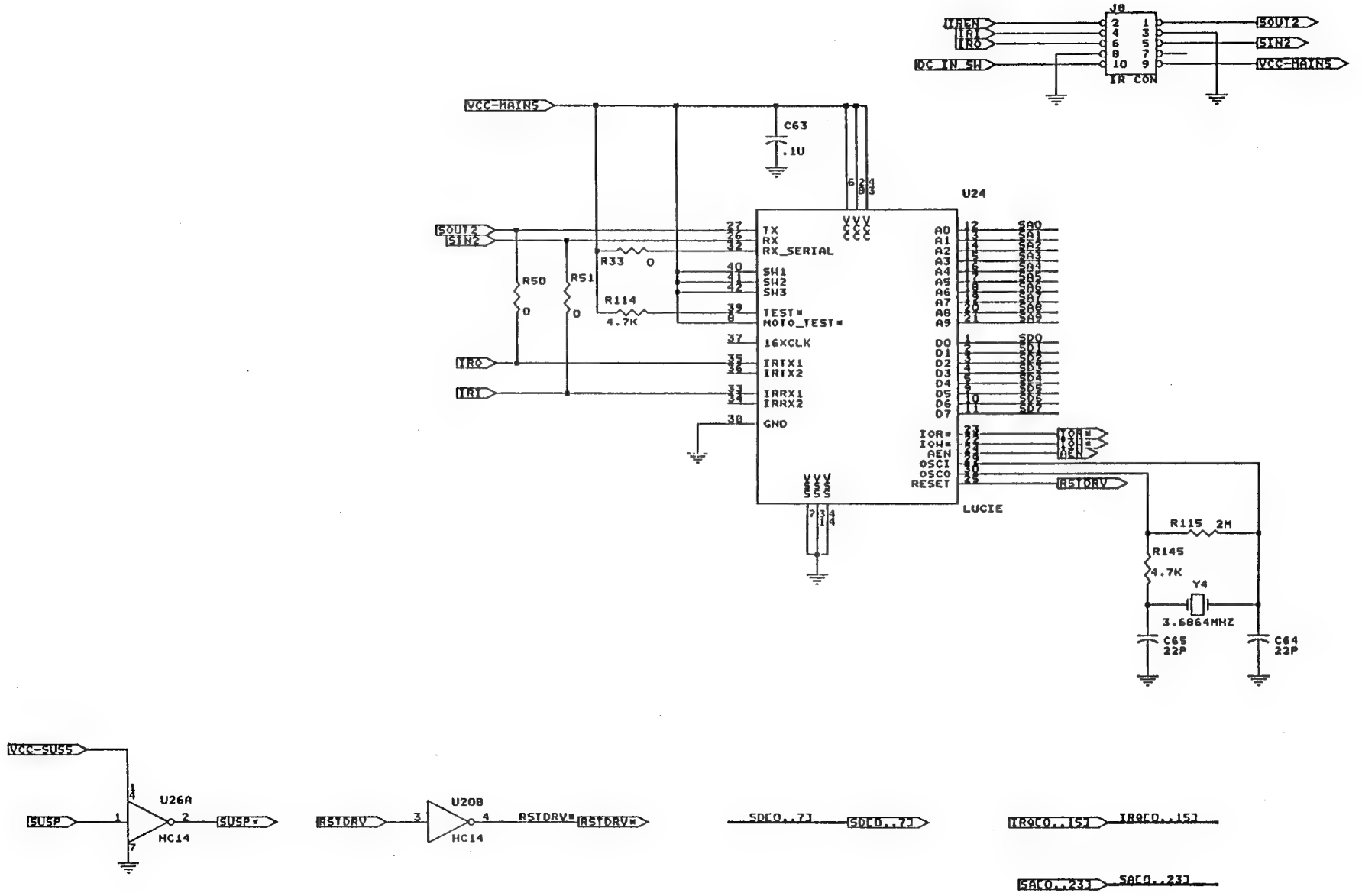

MA2
R73
100K
MA7
R94
100K
VCC-5VS3
MA10
R7
100K
MA5
R92
100K
BCAS#[0..3]
BCAS#[0..3]
BWEN#
BWEN#
BORAS#
BORAS#
B1RAS#
B1RAS#
MA[0..10]
MA[0..10]
MD[0..31]
MD[0..31]
BMA[0..10]
BMA[0..10]
RP7
RCOMN
16
MA0
MA1
MA2
MA3
MA4
MA6
MA8
MA9
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R15
100K#15

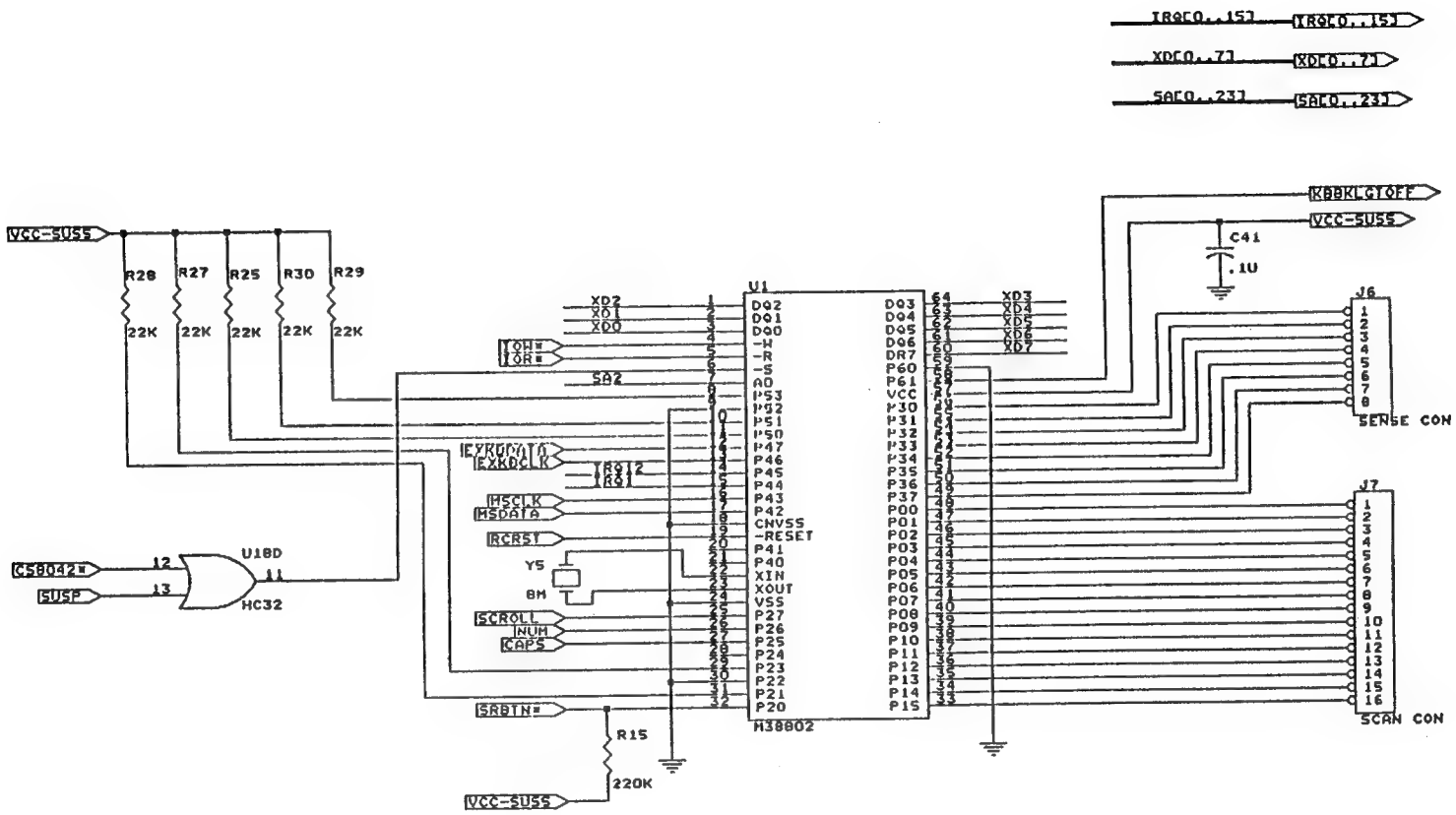

AEN206*
ACK
RESET
VGARST
XIOR
XIOW
IOR*
IOW*
DREQ0
DREQ1
DREQ2
DREQ3
DREQ5
DREQ6
DREQ7
HLDA
IOCHRDY
SCLK
HLDA206
IOCHRDY
SCLK206
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ9
IRQ10
IRQ11
IRQ12
IRQ13
IRQ14
IRQ15
INTA
INTA*
TMRCLK
GATE2
PSRSTB
OSC1
AS
PWRGD
TEST
82C206
MEMR
MEMW
DACK0
DACK1
DACK2
DACK3
DACK5
DACK6
DACK7
HRQ
TC
HRQ206
AEN8
ADSTB8
AEN16
ADSTB16
XA16
XA17
XA18
XA19
XA20
XA21
XA22
XA23
INTR
OUT1
OUT2
REFREQ
OUT2
VSS
VCC
D25
IN4148
R177
2.2K
R175
2.2K
A8
D27
R169
2.2K
A16
D24
R172
10K
R173
1K
R170
2.2K
C70
.1U
C156
4.7U
C155
4700P
R178
0
VCC-206
VCC-MAIN3
VCC-MAIN5
C134
.1U
1DIR
2DIR
/10E
/20E
1A1
1A2
1A3
1A4
1A5
1A6
1A7
1A8
2A1
2A2
2A3
2A4
2A5
2A6
2A7
2A8
1B1
1B2
1B3
1B4
1B5
1B6
1B7
1B8
2B1
2B2
2B3
2B4
2B5
2B6
2B7
2B8
U29
28F001
VPP
WE*
PWD*
OE*
CE*
VCC-FLOSH
C117
.1U
R111
10K
MEMW*
MEMR*
ROMCS*
XD0..7
SA0..23
AC2..31
DACK*0..7
DRQ0..7
IRQ0..15

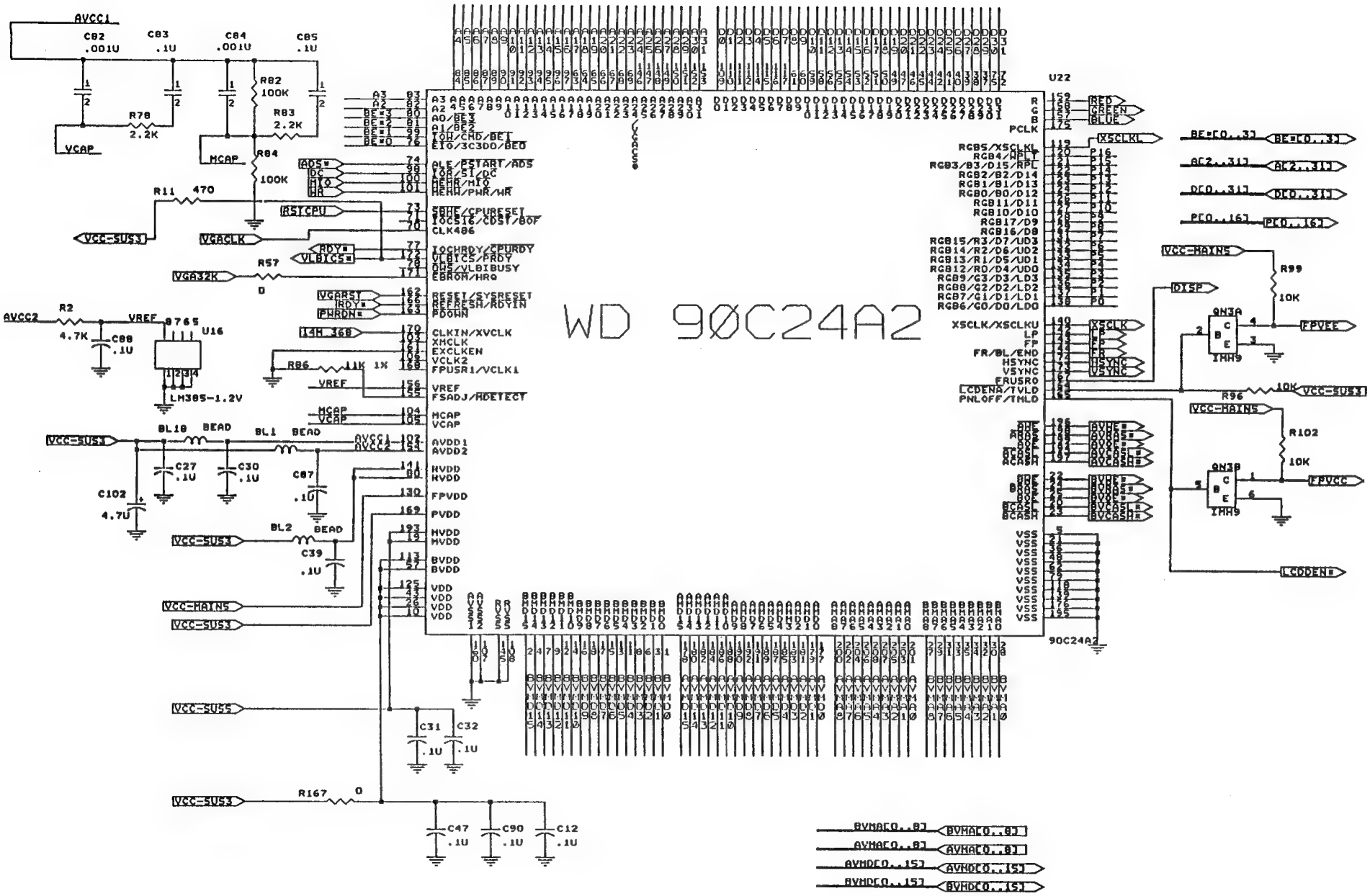


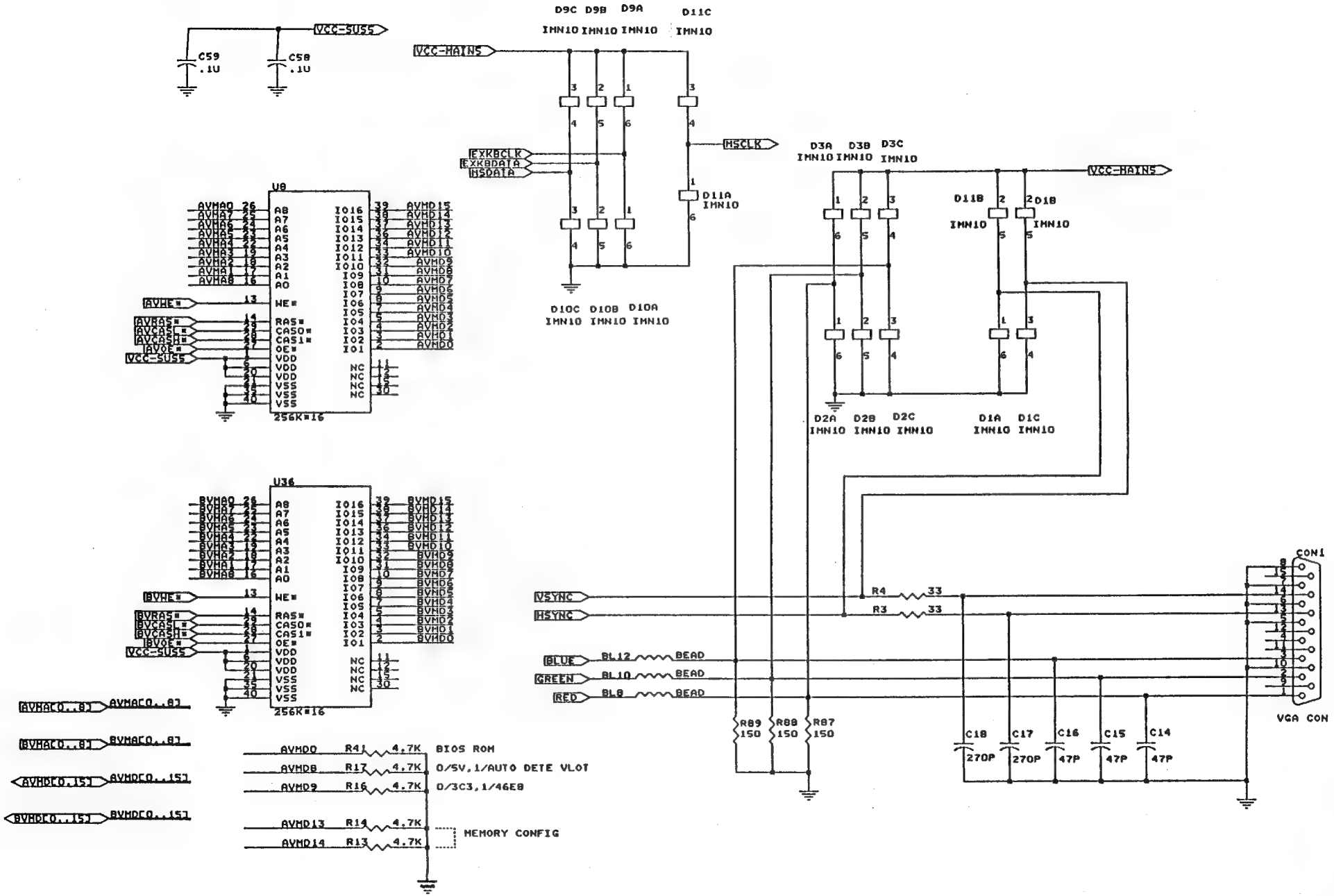
FS1	FS0	:	CPUCLK
1	1	:	80MHZ
1	0	:	66.6MHZ
0	1	:	50MHZ
0	0	:	40MHZ

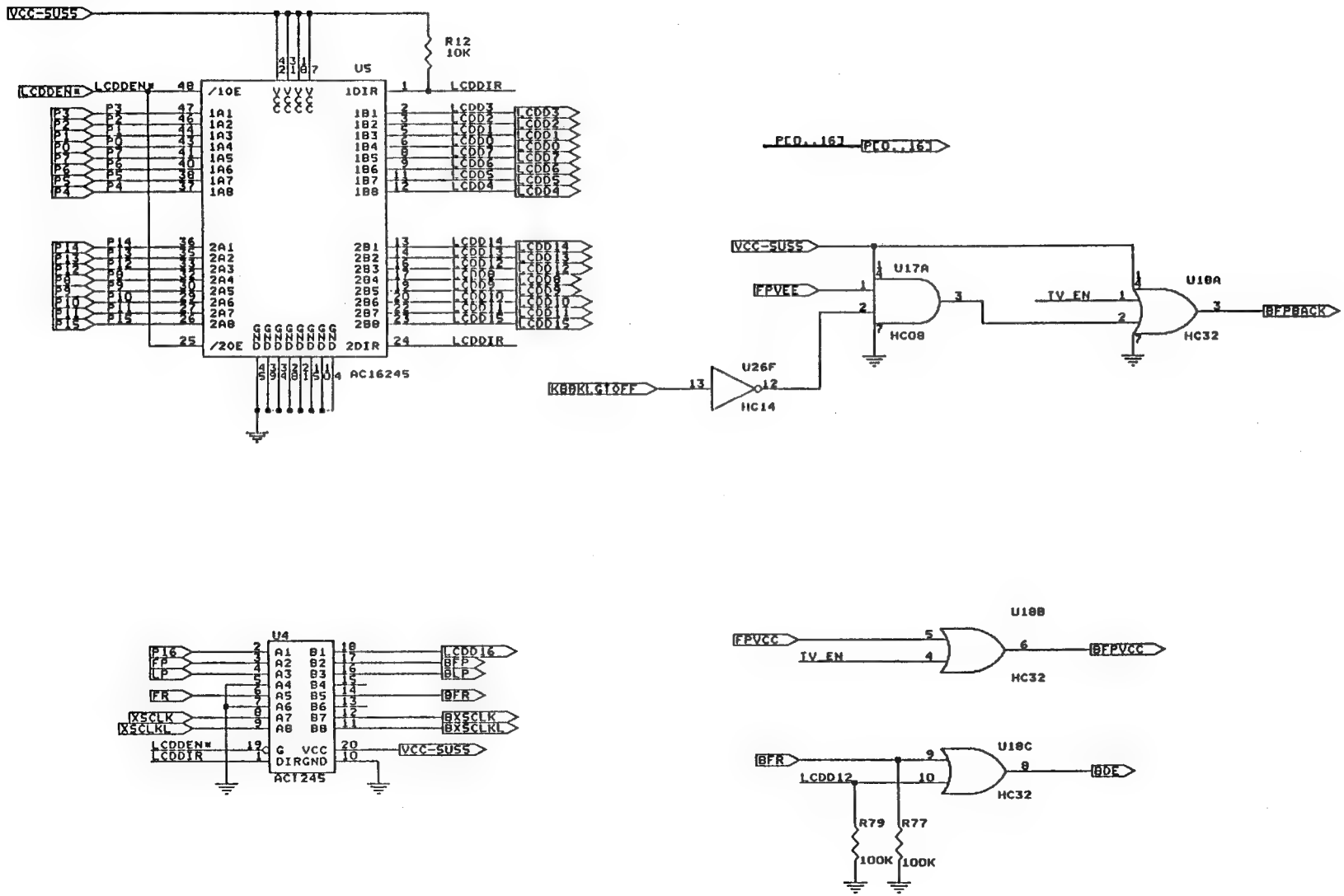


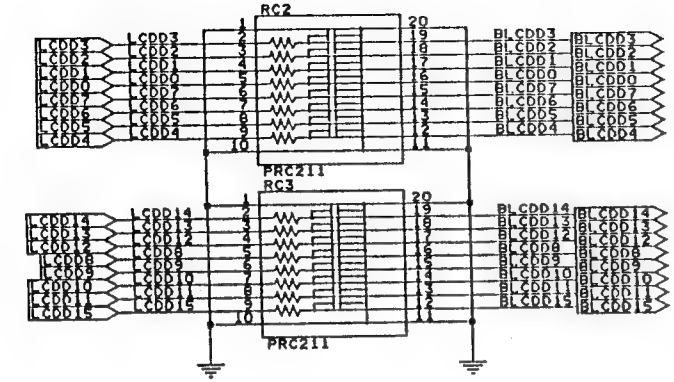

J8
IRAEN
IRI
IRO
DC_IN_SW
SOUT2
SIN2
VCC-MAIN5
IR CON
VCC-MAIN5
C63
.1U
U24
SOUT2
SIN2
R50
0
R51
0
R33 0
R114
4.7K
TX
RX
RX_SERIAL
SW1
SW2
SW3
TEST=
MOTO_TEST=
16XCLK
IRTX1
IRTX2
IRRX1
IRRX2
GND
IRO
IRI
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
D0
D1
D2
D3
D4
D5
D6
D7
IOR=
IOW=
AEN
OSCI
OSCO
RESET
LUCIE
RSTDRV
R115 2M
R145
4.7K
Y4
3.6864MHZ
C65
22P
C64
22P
VCC-5V5S
U26A
5V5P
HC14
5V5P=
RSTDRV
U20B
HC14
RSTDRV=
SDCO..7]
IRQCO..15]
SACO..23]

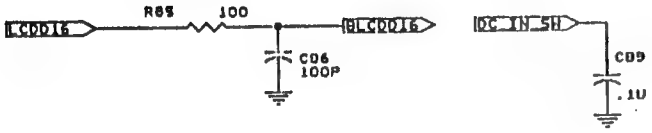

IRQCO..15]
XDCO..7]
SACO..23]
KBBKLGTOFF
VCC-5USS
C41
.1U
R28
R27
R25
R30
R29
22K
U1
XD2
XD1
XD0
IOW#
IOR#
SA2
EXKDATA
EXKDCLK
HSCLK
HSDATA
RCRST
Y5
8M
SCROLL
NUM
CAPS
SRBTN#
R15
220K
VCC-5USS
CS8042#
SUSP
U18D
HC32
H38802
XD3
XD4
XD5
XD6
XD7
J6
SENSE CON
J7
SCAN CON

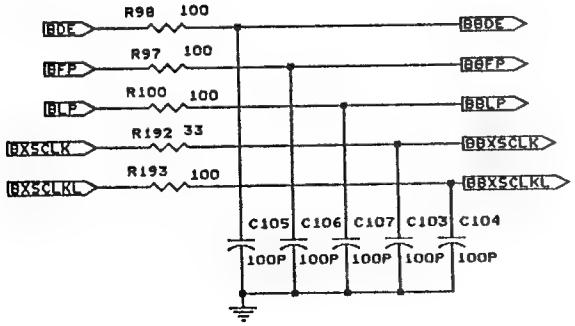

WD 90C24A2
U22
90C24A2
AVCC1
C82 .001U
C83 .1U
C84 .001U
C85 .1U
R82 100K
R83 2.2K
R78 2.2K
VCAP
MCAP
R84 100K
R11 470
VCC-SUS3
VGACLK
RSTCPU
R57 0
VGA32K
AVCC2
R2 4.7K
VREF
C88 .1U
U16
LM385-1.2V
R86 11K 1%
14M 368
BL18 BEAD
BL1 BEAD
C27 .1U
C30 .1U
C87 .1U
C102 4.7U
BL2 BEAD
C39 .1U
VCC-MAIN5
C31 .1U
C32 .1U
R167 0
C47 .1U
C90 .1U
C12 .1U
R99 10K
R96 10K
R102 10K
DISP
FPVEE
FPVCC
LCDDEN
XSCLKL
BE#[0..3]
A[2..31]
D[0..31]
P[0..16]
AVHA[0..8]
AVMA[0..8]
AVHD[0..15]
BVHD[0..15]

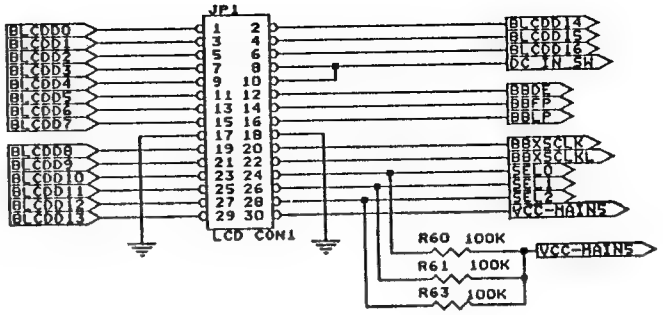

VCC-5V55
C59 .1U
C58 .1U
D9C D9B D9A D11C
IMN10 IMN10 IMN10 IMN10
VCC-MAIN5
HSCLK
EXKBCLK
EXKBDATA
HSDATA
D11A IMN10
D10C D10B D10A
IMN10 IMN10 IMN10
D3A D3B D3C
IMN10 IMN10 IMN10
VCC-MAIN5
D11B IMN10
D1B IMN10
D2A D2B D2C
IMN10 IMN10 IMN10
D1A D1C
IMN10 IMN10
U8
AVMA0 AVMA1 AVMA2 AVMA3 AVMA4 AVMA5 AVMA6 AVMA7 AVMA8
AVHE#
AVRAS#
AVCASL#
AVCASH#
AVOE#
VCC-5V55
A8 A7 A6 A5 A4 A3 A2 A1 A0
WE# RAS# CAS0# CAS1# OE#
VDD VDD VDD VSS VSS VSS
I016 I015 I014 I013 I012 I011 I010 I09 I08 I07 I06 I05 I04 I03 I02 I01
NC NC NC NC
AVMD15 AVMD14 AVMD13 AVMD12 AVMD11 AVMD10 AVMD9 AVMD8 AVMD7 AVMD6 AVMD5 AVMD4 AVMD3 AVMD2 AVMD1 AVMD0
256K*16
U36
BVMA0 BVMA1 BVMA2 BVMA3 BVMA4 BVMA5 BVMA6 BVMA7 BVMA8
BVHE#
BVRAS#
BVCASL#
BVCASH#
BVOE#
VCC-5V55
BVMD15 BVMD14 BVMD13 BVMD12 BVMD11 BVMD10 BVMD9 BVMD8 BVMD7 BVMD6 BVMD5 BVMD4 BVMD3 BVMD2 BVMD1 BVMD0
256K*16
VSYNC
HSYNC
BLUE
GREEN
RED
BL12 BL10 BL8
BEAD
R4 33
R3 33
R89 150
R88 150
R87 150
C18 270P
C17 270P
C16 47P
C15 47P
C14 47P
CON1
VGA CON
AVMA0..8
BVMA0..8
AVMD0..15
BVMD0..15
AVMD0 R41 4.7K BIOS ROM
AVMD8 R17 4.7K 0/5V,1/AUTO DETE VLOT
AVMD9 R16 4.7K 0/3C3,1/46E8
AVMD13 R14 4.7K
AVMD14 R13 4.7K
MEMORY CONFIG


VCC-5USS
R12
10K
U5
LCDDEN#
LCDDEN#
/10E
1DIR
LCDDIR
1A1
1A2
1A3
1A4
1A5
1A6
1A7
1A8
1B1
1B2
1B3
1B4
1B5
1B6
1B7
1B8
LCDD3
LCDD2
LCDD1
LCDD0
LCDD7
LCDD6
LCDD5
LCDD4
2A1
2A2
2A3
2A4
2A5
2A6
2A7
2A8
2B1
2B2
2B3
2B4
2B5
2B6
2B7
2B8
LCDD14
LCDD13
LCDD12
LCDD8
LCDD9
LCDD10
LCDD11
LCDD15
/20E
2DIR
LCDDIR
AC16245
P[0..16]
P[0..16]
VCC-5USS
U17A
FPVEE
HC08
IV_EN
U18A
HC32
BFPBACK
KBBKLGIOFF
U26F
HC14
U4
P16
FP
LP
FR
XSCLK
XSCLKL
LCDDEN#
LCDDIR
G
VCC
DIRGND
ACT245
LCDD16
BFP
BLP
BFR
BXSCLK
BXSCLKL
VCC-5USS
U18B
FPVCC
IV_EN
BFPVCC
HC32
U18C
BFR
LCDD12
BDE
HC32
R79
R77
100K
100K

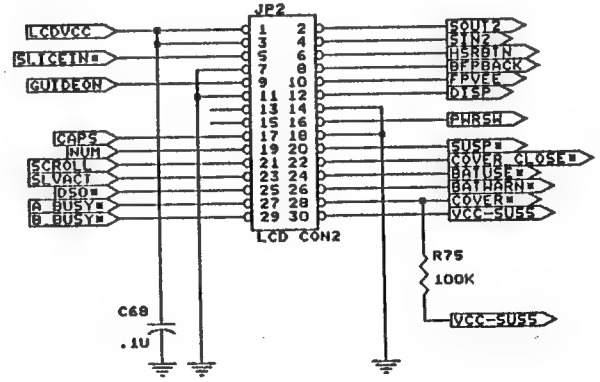


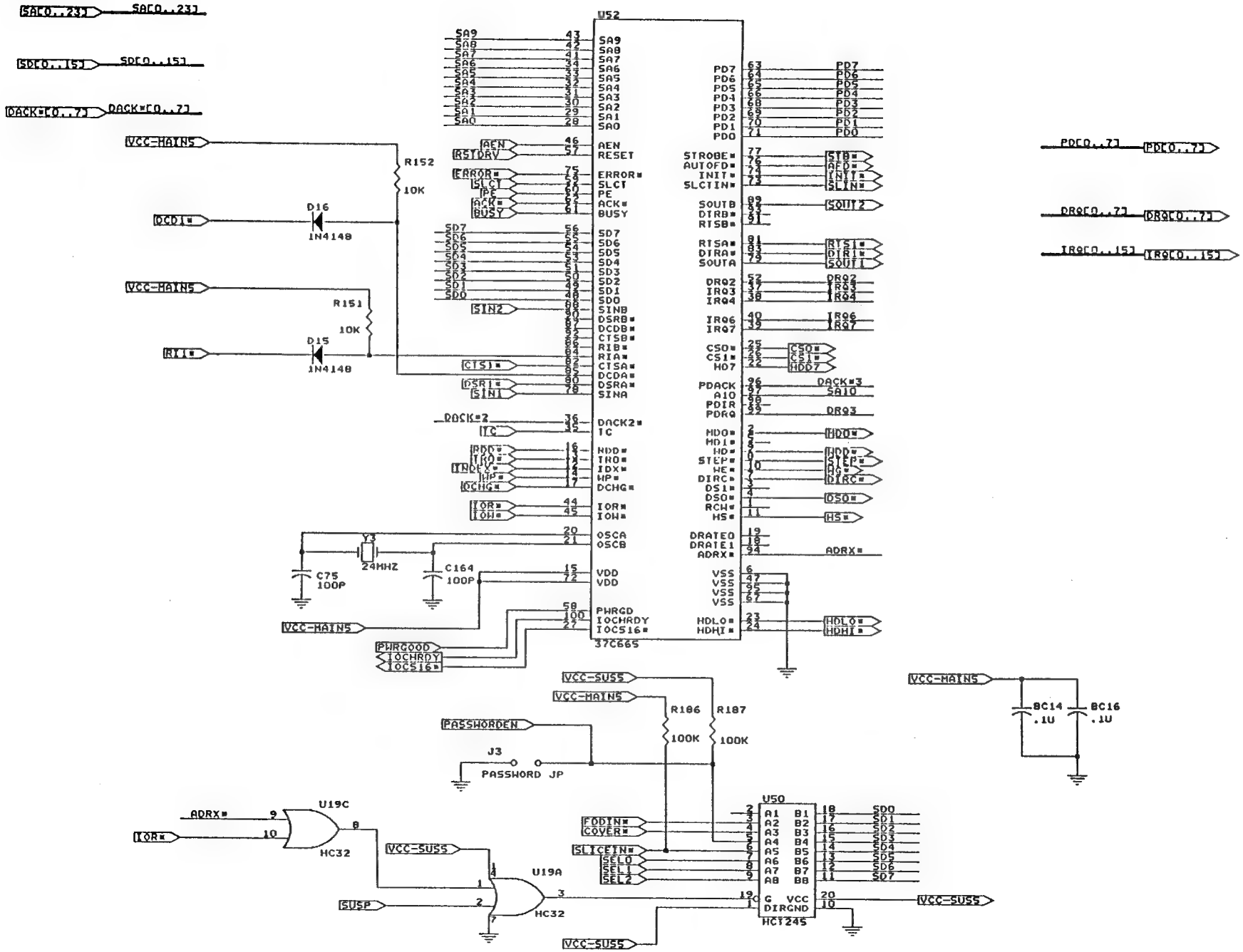


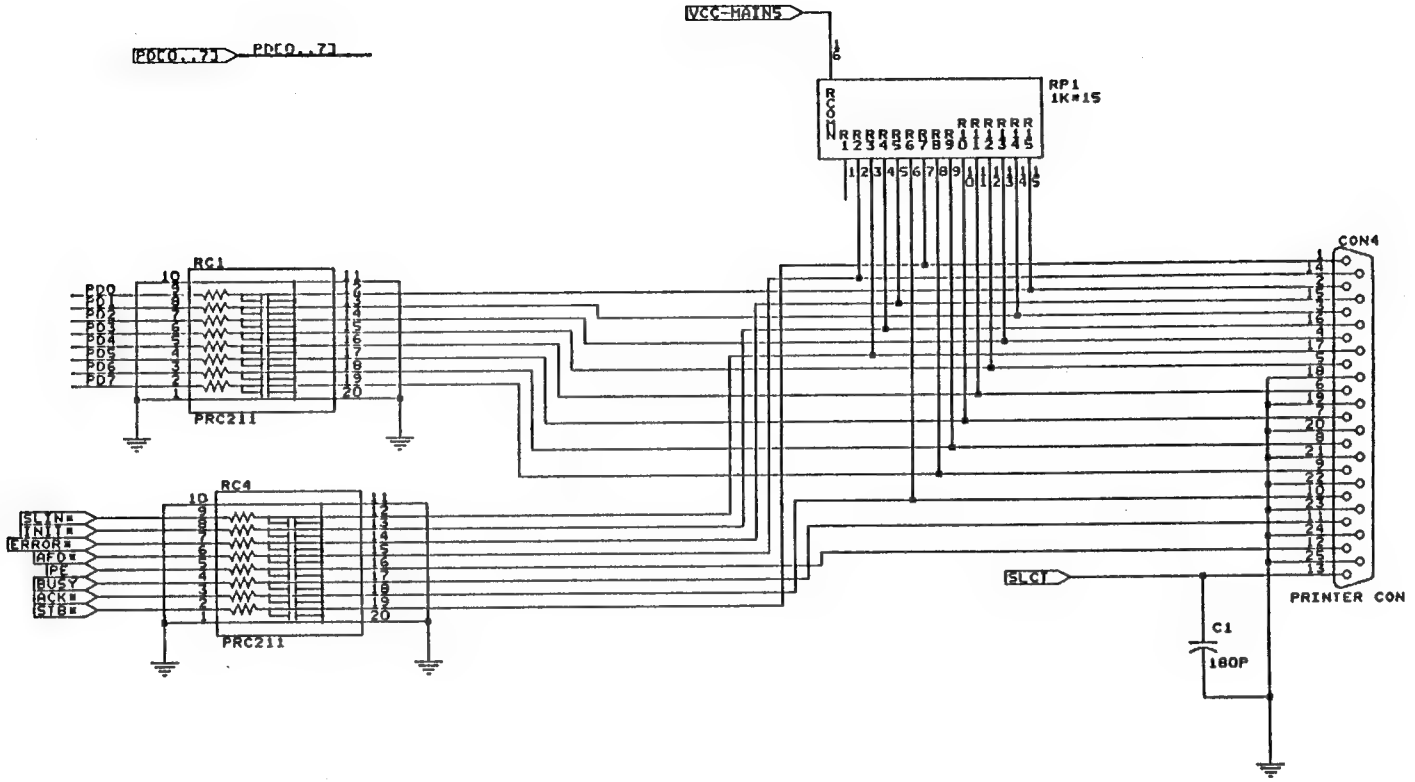


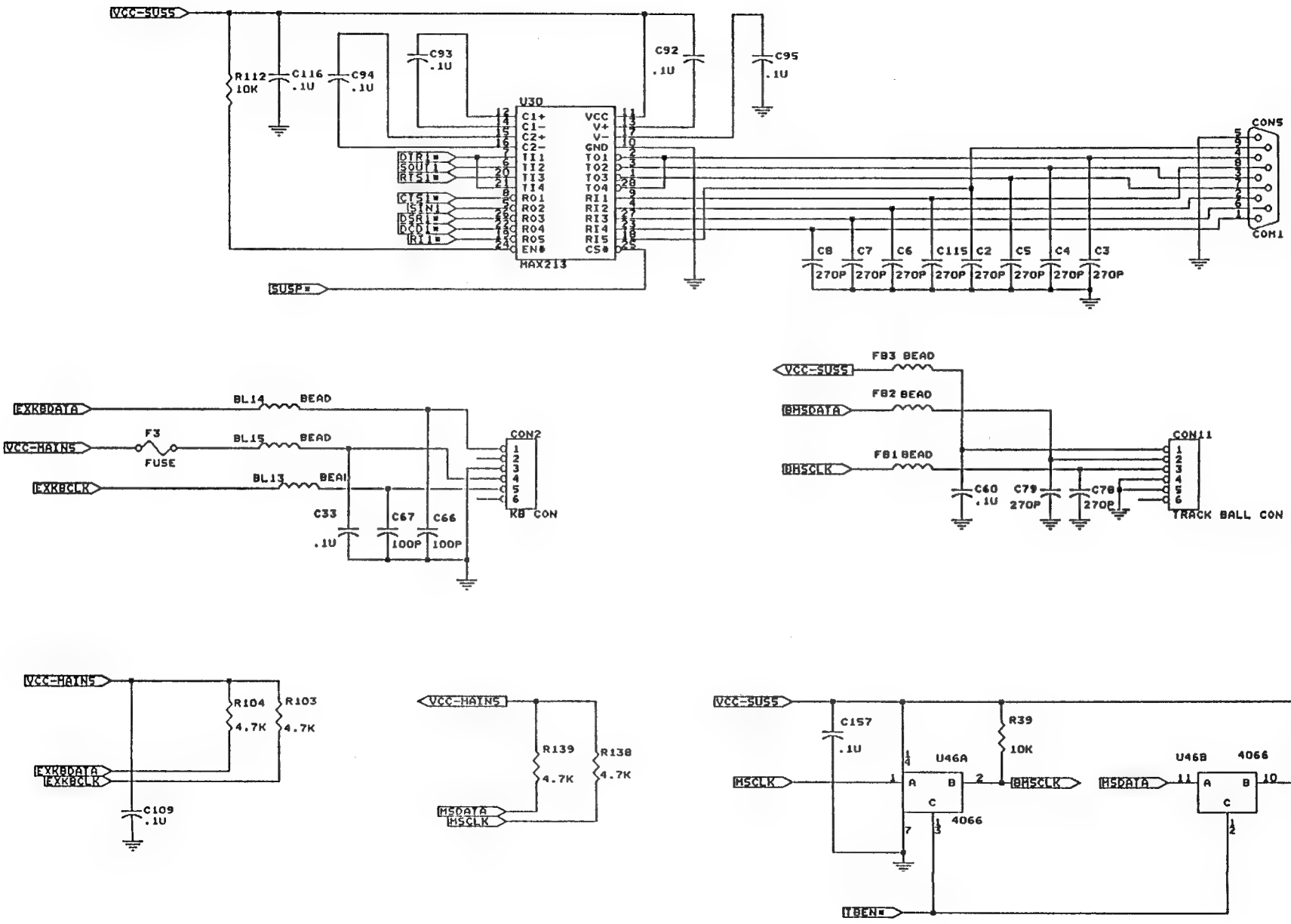


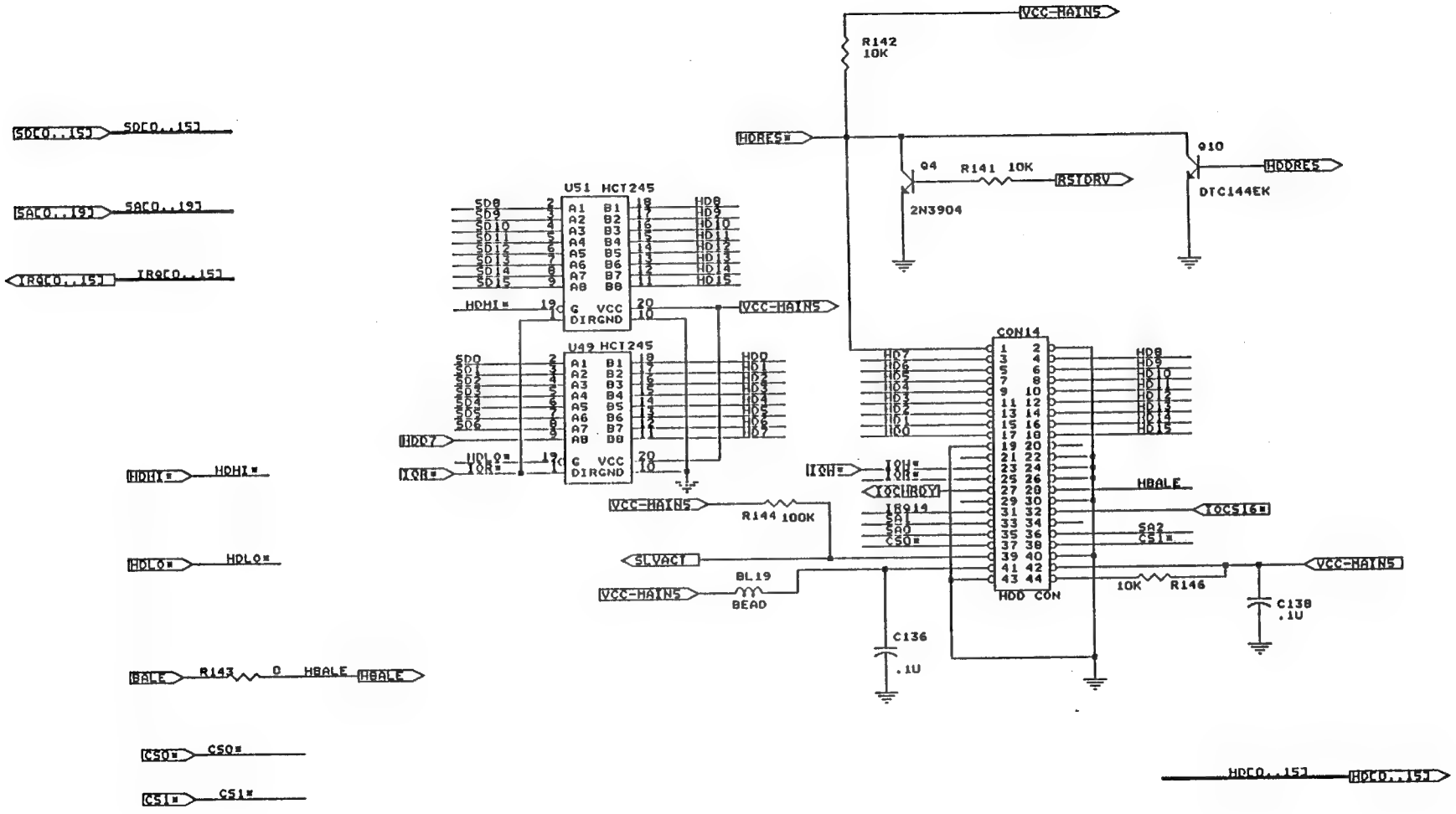
	SEL0	SEL1	SEL2
DSTN :	1	1	1
MONO :	0	1	1
9BIT TFT :	1	0	1
12BIT TFT :	0	0	1
18BIT TFT :	0	0	0

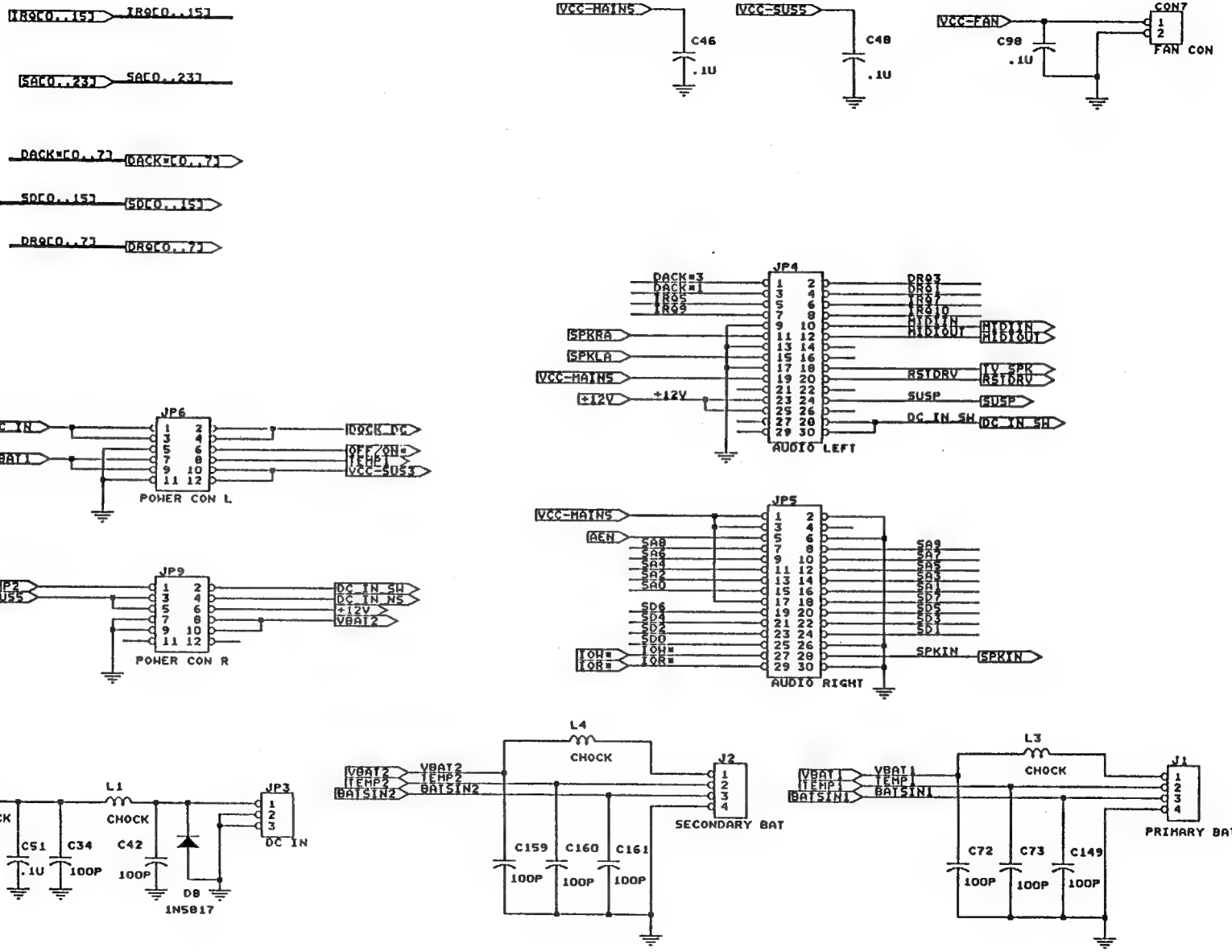


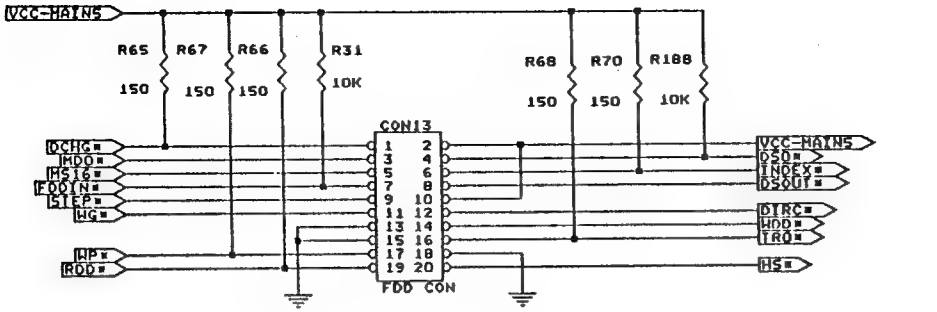

SAC0..23]
SDC0..15]
DACK#C0..7]
VCC-MAIN5
R152
10K
D16
IN4148
DCD1#
R151
10K
D15
IN4148
RI1#
U52
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
AEN
RSTDRV
ERROR#
SLCT
PE
ACK#
BUSY
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
SIN2
DSRB#
DCDB#
CTSB#
RIB#
RIA#
CTS1#
CTSA#
DCDA#
DSRA#
SIN1
SINA
DACK#2
DACK2#
TC
NDD#
IRQ#
IDX#
HP#
DCHG#
IOR#
IOW#
OSCA
OSCB
Y3
24MHZ
C75
100P
C164
100P
VDD
VDD
PWRGD
IOCHRDY
IOCS16#
37C665
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0
STROBE#
AUTOFD#
INIT#
SLCTIN#
SOUTB
DTRB#
RTSB#
RTSA#
DTRA#
SOUTA
DRQ2
IRQ3
IRQ4
IRQ6
IRQ7
CS0#
CS1#
HD7
PDACK
A10
PDIR
PDRQ
MDO#
MDI#
HD#
STEP#
WE#
DIRC#
DS1#
DS0#
RCH#
HS#
DRATE0
DRATE1
ADRX#
VSS
VSS
VSS
VSS
HDLO#
HDHI#
PDC0..7]
DRQC0..7]
IRQC0..15]
STB#
AFD#
INIT#
SLIN#
SOUT2
RTS1#
DTR1#
SOUT1
DRQ2
IRQ3
IRQ4
IRQ6
IRQ7
CS0#
CS1#
HDD7
DACK#3
SA10
DRQ3
HDO#
HDD#
STEP#
DIRC#
DS0#
HS#
ADRX#
PASSWORDEN
J3
PASSWORD JP
R186
100K
R187
100K
VCC-SUS5
VCC-MAIN5
BC14
.1U
BC16
.1U
U19C
ADRX#
IOR#
HC32
U19A
SUSP
HC32
FDDIN#
COVER#
SLICEIN#
SEL0
SEL1
SEL2
U50
A1 B1
A2 B2
A3 B3
A4 B4
A5 B5
A6 B6
A7 B7
A8 B8
G VCC
DIRGND
HCT245
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
PWRGOOD
IOCHRDY
IOCS16#

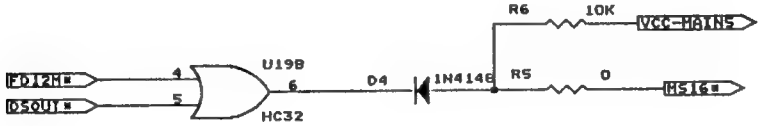

VCC=MAIN5
PD[0..7]
PD[0..7]
RP1
1K*15
RC1
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PRC211
RC4
SLIN*
INIT*
ERROR*
AFD*
PE
BUSY
ACK*
STB*
PRC211
CON4
SLCT
C1
180P
PRINTER CON

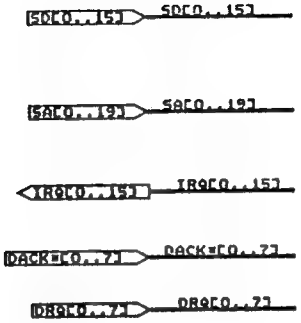

VCC-5USS
R112 10K
C116 .1U
C94 .1U
C93 .1U
C92 .1U
C95 .1U
U30
MAX213
C1+
C1-
C2+
C2-
VCC
V+
V-
GND
DTR1
SOUT1
RTS1
CTS1
ISIN1
DSR1
DCD1
RI1
TO1
TO2
TO3
TO4
RI1
RI2
RI3
RI4
RI5
CS
EN
SUSP
CON5
COM1
C8 270P
C7 270P
C6 270P
C115 270P
C2 270P
C5 270P
C4 270P
C3 270P
EXKBDATA
VCC-MAIN5
EXKBCLK
BL14 BEAD
BL15 BEAD
BL13 BEAD
F3
FUSE
C33 .1U
C67 100P
C66 100P
CON2
KB CON
FB3 BEAD
FB2 BEAD
FB1 BEAD
BHSDATA
BHSCLK
C60 .1U
C79 270P
C78 270P
CON11
TRACK BALL CON
R104 4.7K
R103 4.7K
C109 .1U
R139 4.7K
R138 4.7K
MSDATA
MSCLK
C157 .1U
U46A
4066
R39 10K
R40 10K
U46B
HSDATA
TBEN

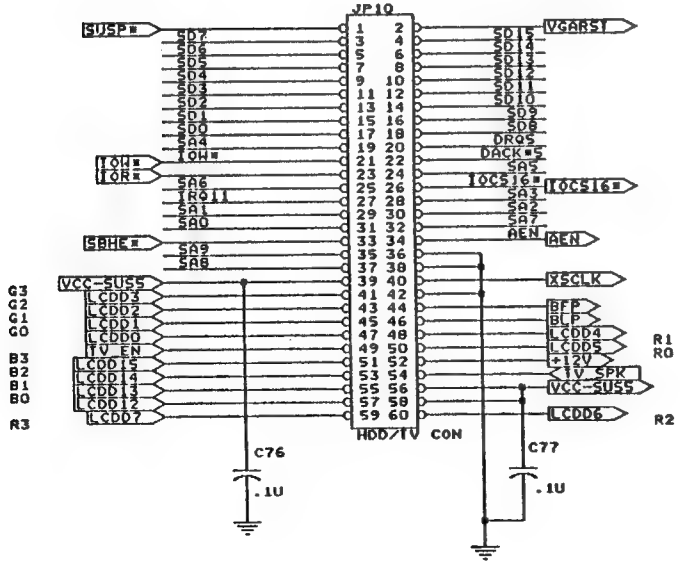

SDC0..15
SDC0..15
SAC0..19
SAC0..19
IRQC0..15
IRQC0..15
HDHI#
HDHI#
HDLO#
HDLO#
BALE
R143
0
HBALE
HBALE
CS0#
CS0#
CS1#
CS1#
U51 HCT245
U49 HCT245
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
HD8
HD9
HD10
HD11
HD12
HD13
HD14
HD15
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
G
VCC
DIRGND
VCC-MAIN5
HDRES#
R142
10K
Q4
2N3904
R141 10K
RSTDRV
Q10
DTC144EK
HDDRES
CON14
HDD CON
IOR#
IOW#
IOCHRDY
IRQ14
SA1
SA0
CS0#
SA2
CS1#
HBALE
IOCS16#
SLVACT
R144 100K
BL19
BEAD
C136
.1U
R146
10K
C138
.1U
HDC0..15
HDC0..15


IRQCO..15]
SACO..23]
DACK#CO..7]
SDCO..15]
DRQCO..7]
VCC-MAINS
C46
.1U
VCC-SUS5
C48
.1U
VCC-FAN
C98
.1U
CON7
FAN CON
JP4
DACK#3
DACK#1
IRQ5
IRQ9
SPKRA
SPKLA
VCC-MAINS
+12V
DRQ3
DRQ1
IRQ7
IRQ10
HIDIN
HIDOUT
RSTDRV
SUSP
DC_IN_SW
5V_SPK
AUDIO LEFT
JP6
DC_IN
VBAT1
DOCK_DC
OFF/ON#
TEMP1
VCC-SUS3
POWER CON L
JP9
TEMP2
VCC-SUS5
DC_IN_SW
DC_IN_NS
+12V
VBAT2
POWER CON R
JP5
VCC-MAINS
AEN
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IOW#
IOR#
SPKIN
AUDIO RIGHT
DC_IN
D18
SFPB-74
L2
CHOCK
L1
CHOCK
C51
.1U
C34
100P
C42
100P
D8
1N5817
JP3
DC IN
L4
CHOCK
VBAT2
TEMP2
BATSIN2
J2
SECONDARY BAT
C159
C160
C161
100P
L3
CHOCK
VBAT1
TEMP1
BATSIN1
J1
PRIMARY BAT
C72
C73
C149

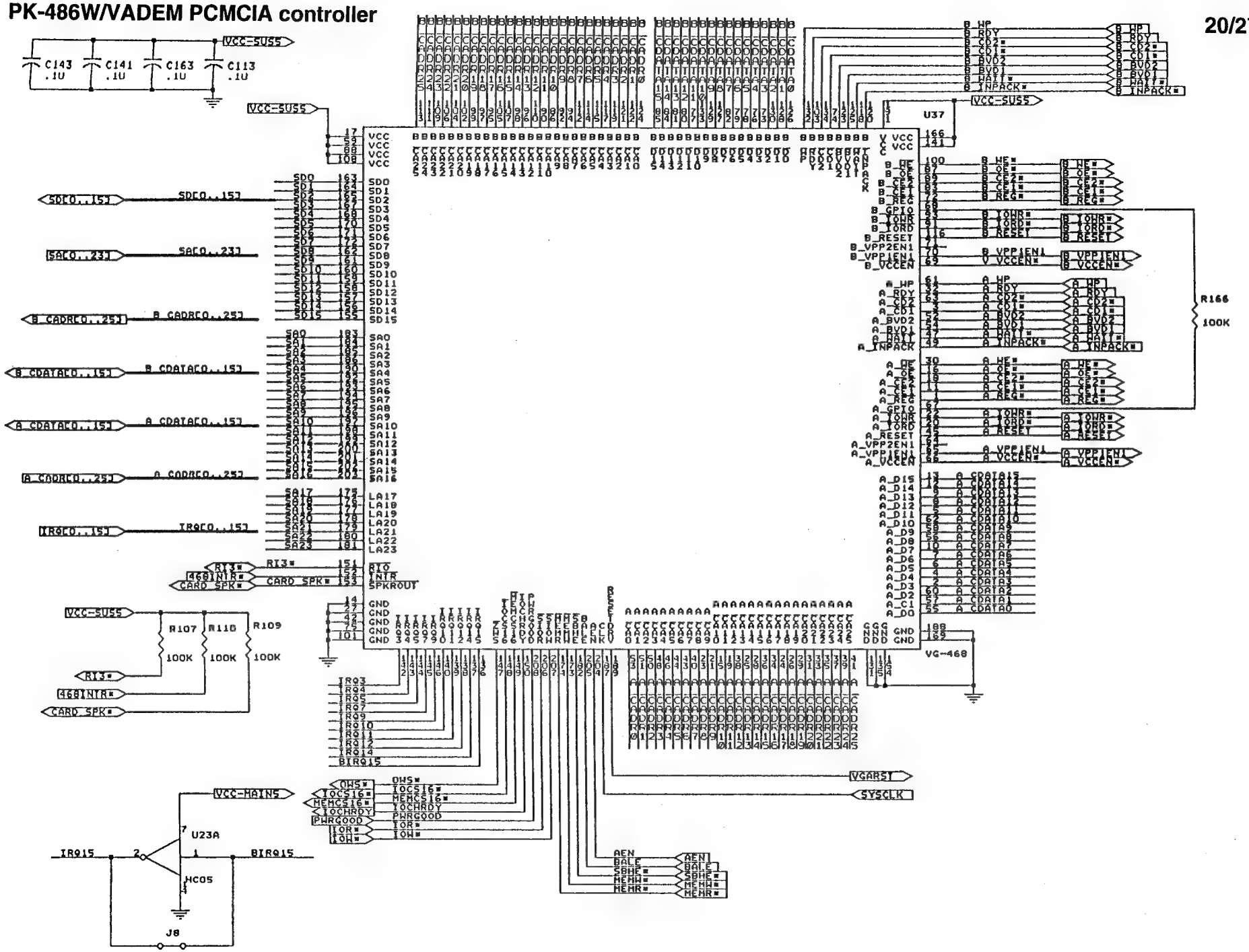

VCC-HAINS
R65
150
R67
150
R66
150
R31
10K
R68
150
R70
150
R188
10K
CON13
DCHG■
MDO■
MS16■
FDQIN■
STEP■
WG■
WP■
RDD■
VCC-HAINS
DSO■
INDEX■
DSOUT■
DIRC■
HDD■
TRO■
HS■
FDD CON


R6
10K
VCC-HAINS
FDI2M■
DSOUT■
U19B
HC32
D4
1N4148
R5
0
HS16■

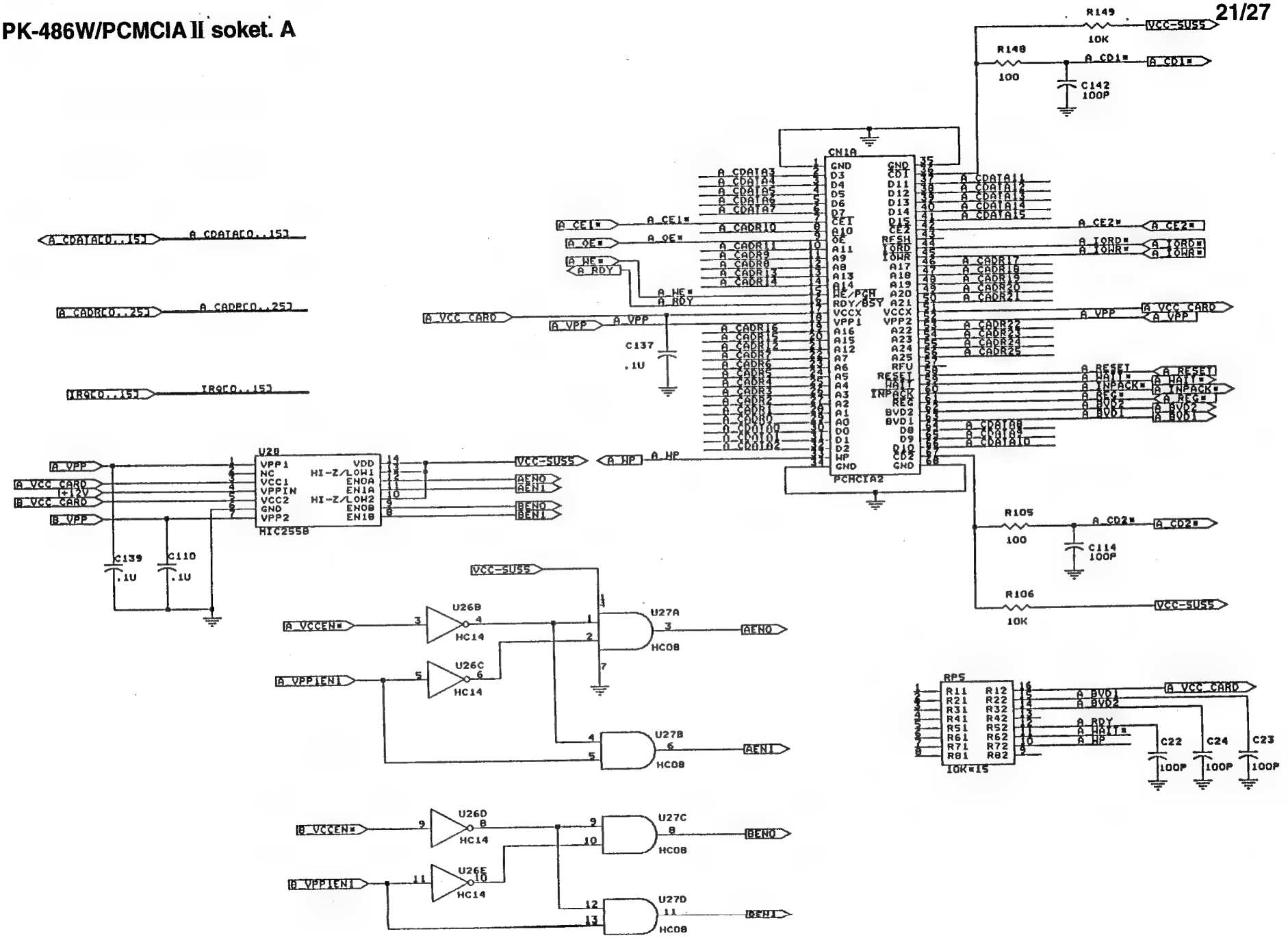

SDC0..15]
SDC0..15]
SAC0..19]
SAC0..19]
IRQC0..15]
IRQC0..15]
DACK■C0..7]
DACK■C0..7]
DRQC0..7]
DRQC0..7]

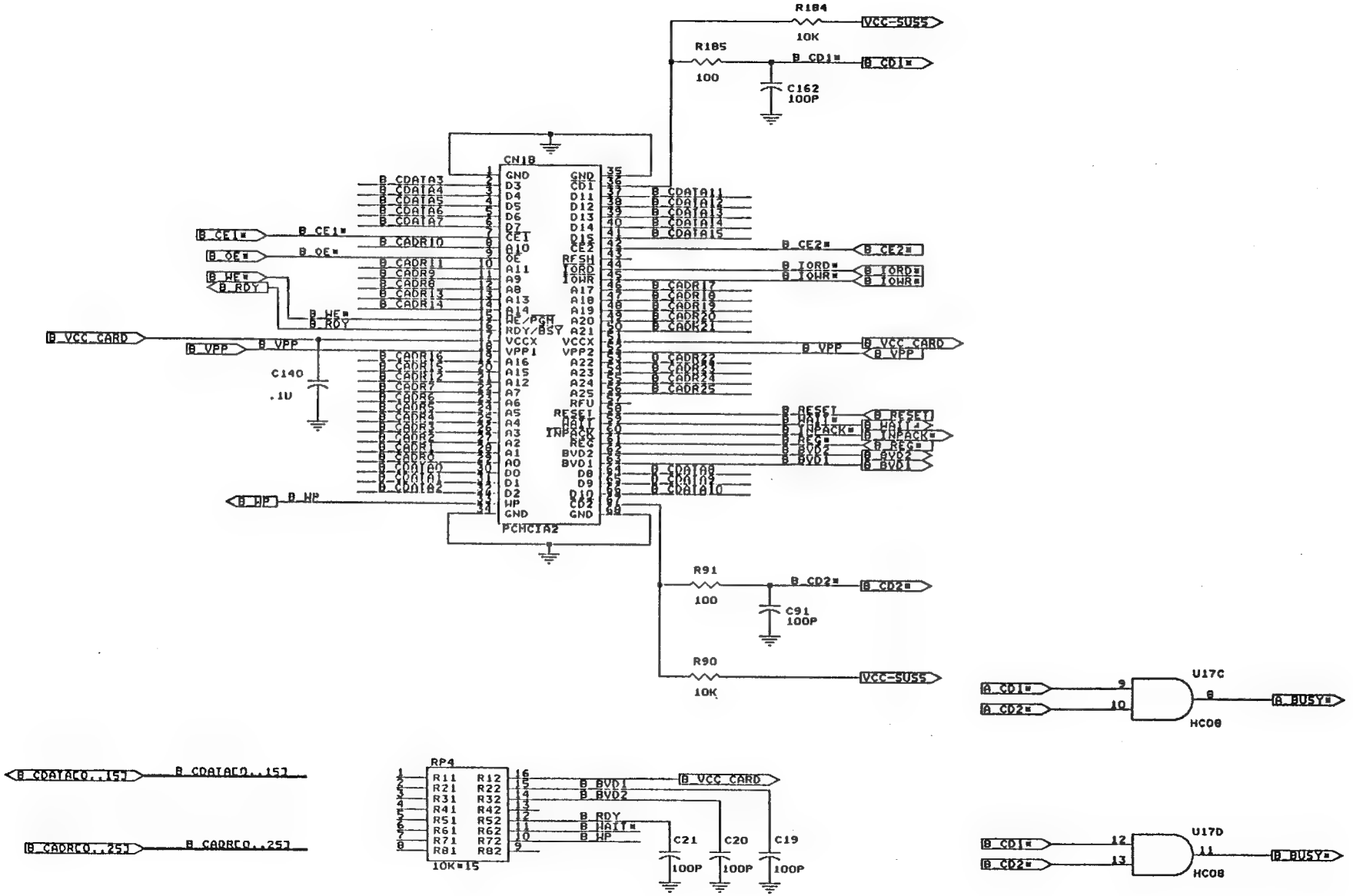

JP10
SUSP■
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
RST
IOH■
IOW■
IOR■
SA6
IRQ11
SA1
SA0
SBHE■
SA9
SA8
VCC-SUS5
G3
G2
G1
G0
B3
B2
B1
B0
R3
LCDD3
LCDD2
LCDD1
LCDD0
TV_EN
LCDD15
LCDD14
LCDD13
LCDD12
LCDD7
SD15
SD14
SD13
SD12
SD11
SD10
SD9
SD8
DRQ5
DACK■5
SA5
IOCS16■
SA4
SA3
SA2
SA7
AEN
VGARST
IOCS16■
AEN
XSCLK
BFP
BLP
LCDD4
LCDD5
+12V
1V_SPK
VCC-SUS5
LCDD6
R1
R0
R2
HDD/TV CON
C76
.1U
C77
.1U

PK-486W/VADEM PCMCIA controller

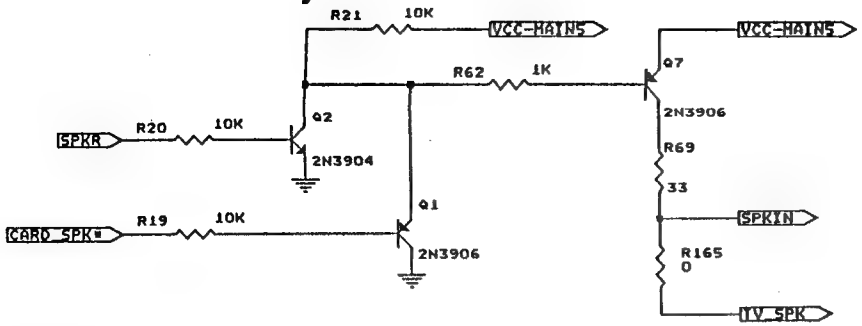


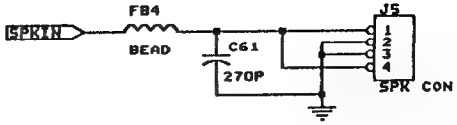
PK-486W/PCMCIA II soket. A

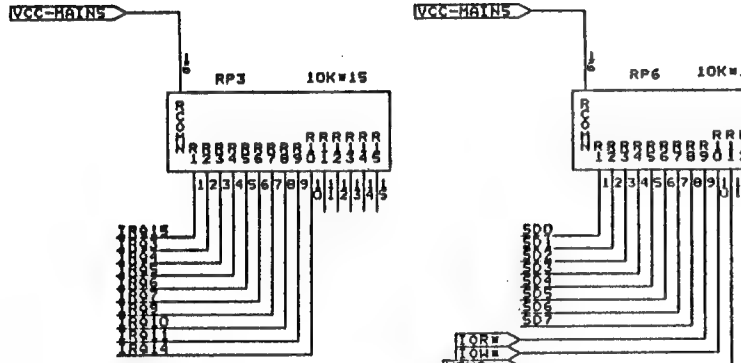


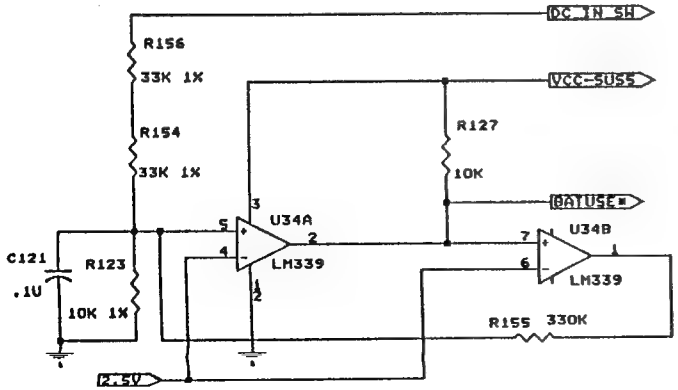

R184
10K
VCC-5USS
R185
100
B_CD1
C162
100P
CN1B
PCMCIA2
B_CDATA3
B_CDATA4
B_CDATA5
B_CDATA6
B_CDATA7
B_CE1
B_CADR10
B_OE
B_CADR11
B_CADR9
B_CADR8
B_CADR13
B_CADR14
B_WE
B_RDY
B_VCC_CARD
B_VPP
C140
.1U
B_CADR16
B_CADR15
B_CADR12
B_CADR7
B_CADR6
B_CADR5
B_CADR4
B_CADR3
B_CADR2
B_CADR1
B_CADR0
B_CDATA0
B_CDATA1
B_CDATA2
B_HP
B_CDATA11
B_CDATA12
B_CDATA13
B_CDATA14
B_CDATA15
B_CE2
B_IORD
B_IOWR
B_CADR17
B_CADR18
B_CADR19
B_CADR20
B_CADR21
B_CADR22
B_CADR23
B_CADR24
B_CADR25
B_RESET
B_WAIT
B_INPACK
B_REG
B_BVD2
B_BVD1
B_CDATA8
B_CDATA9
B_CDATA10
R91
100
B_CD2
C91
100P
R90
10K
VCC-5USS
U17C
HC08
A_CD1
A_CD2
A_BUSY
B_CDATAC0..15]
B_CADRC0..25]
RP4
10K*15
B_BVD1
B_BVD2
B_RDY
B_WAIT
B_HP
C21
C20
C19
100P
U17D
B_BUSY

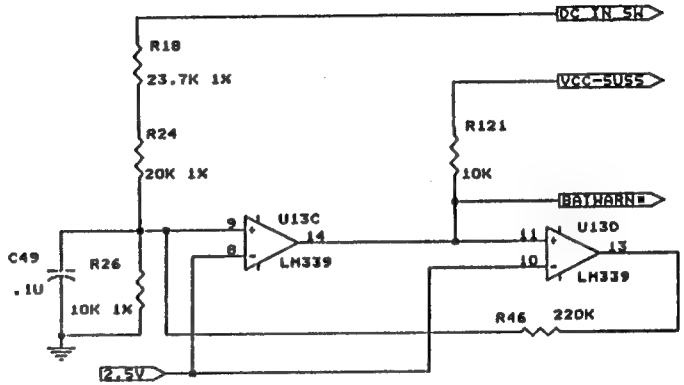
PK-486W/SPK/Battery status circuit

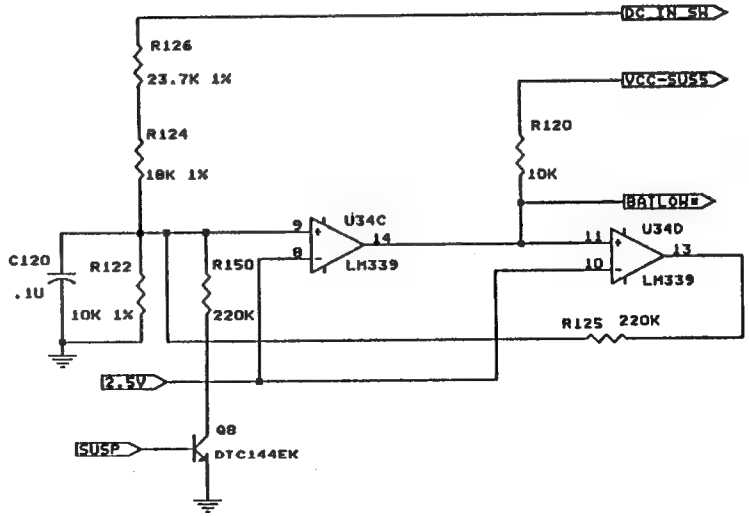




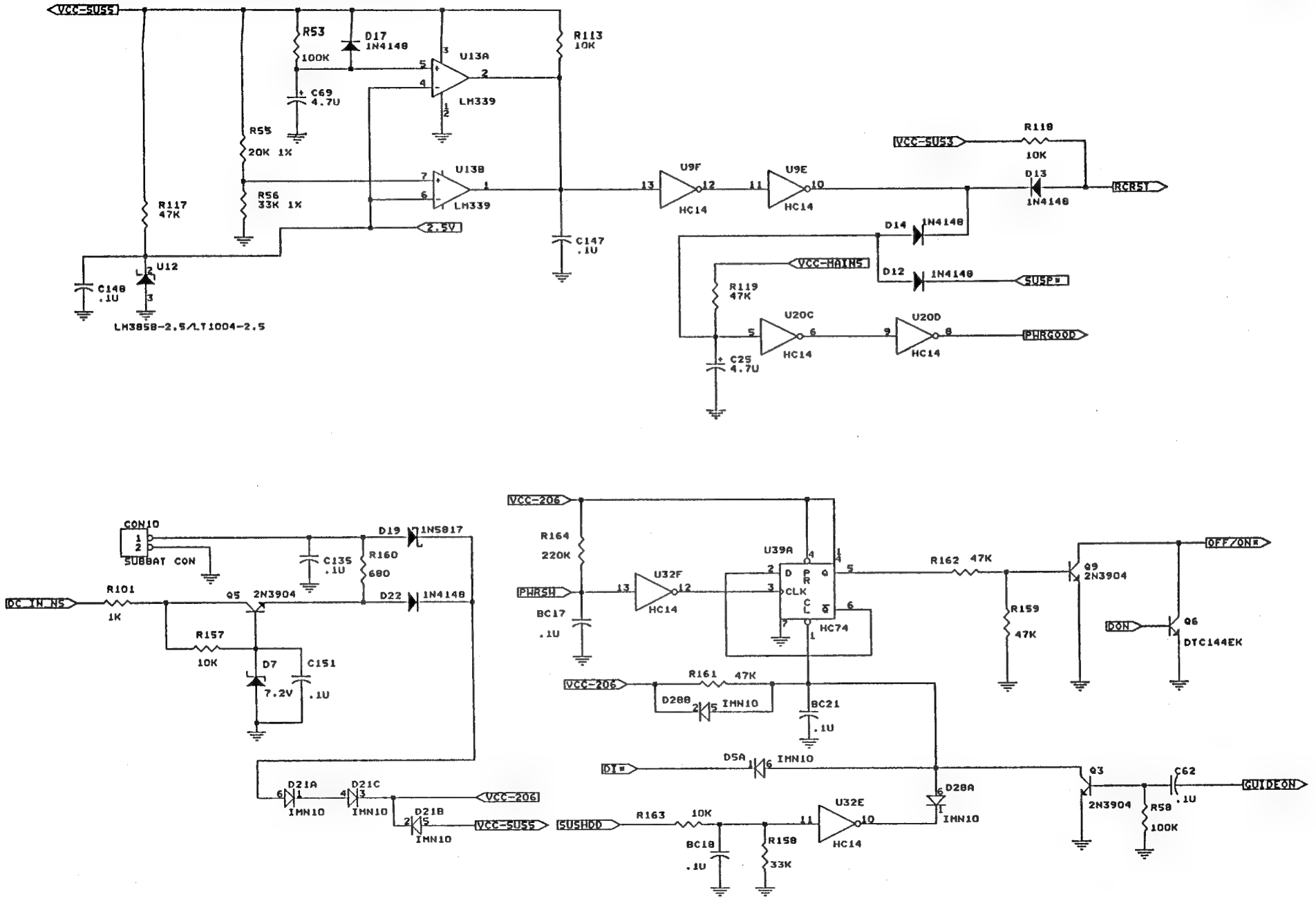


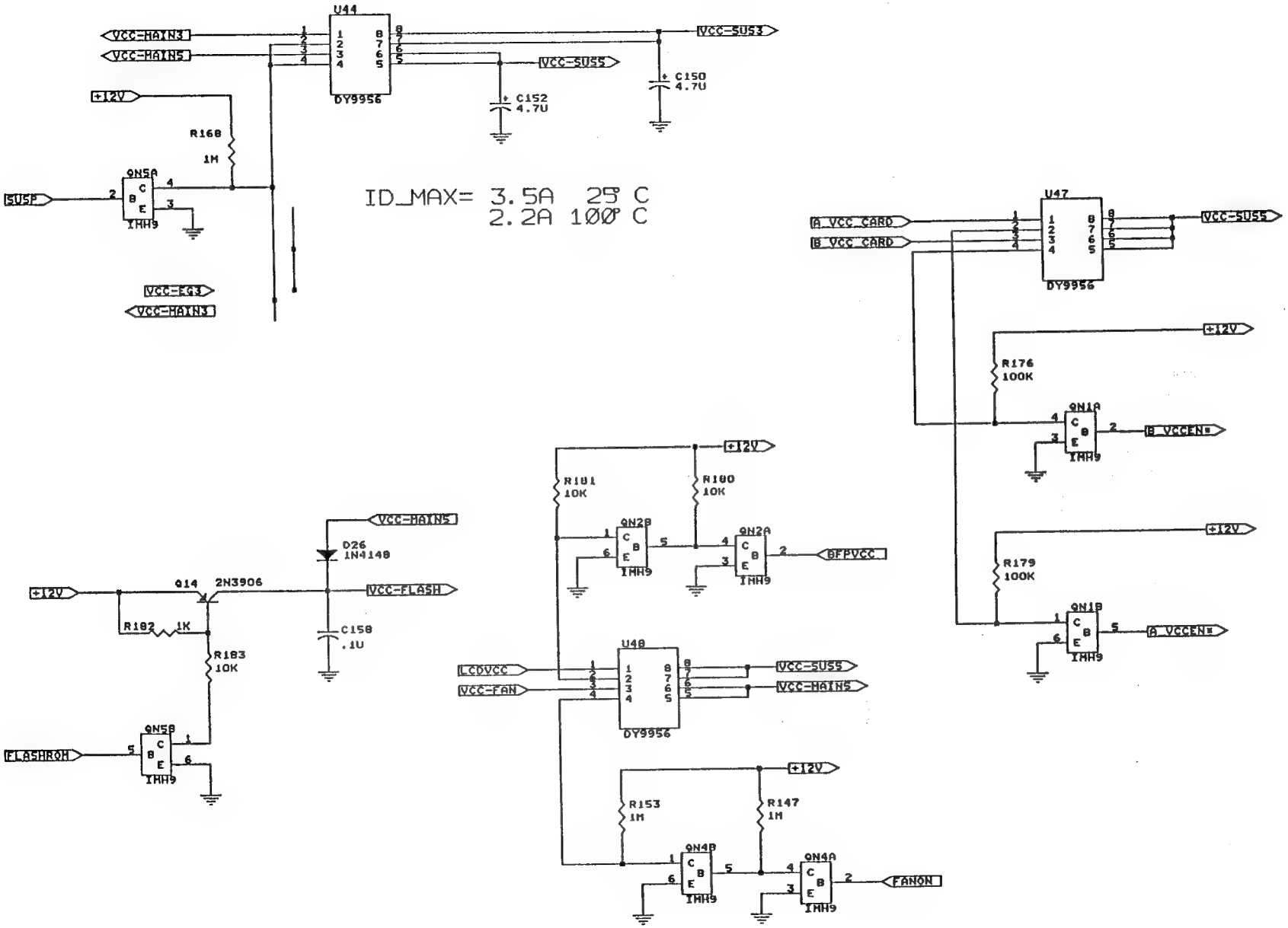


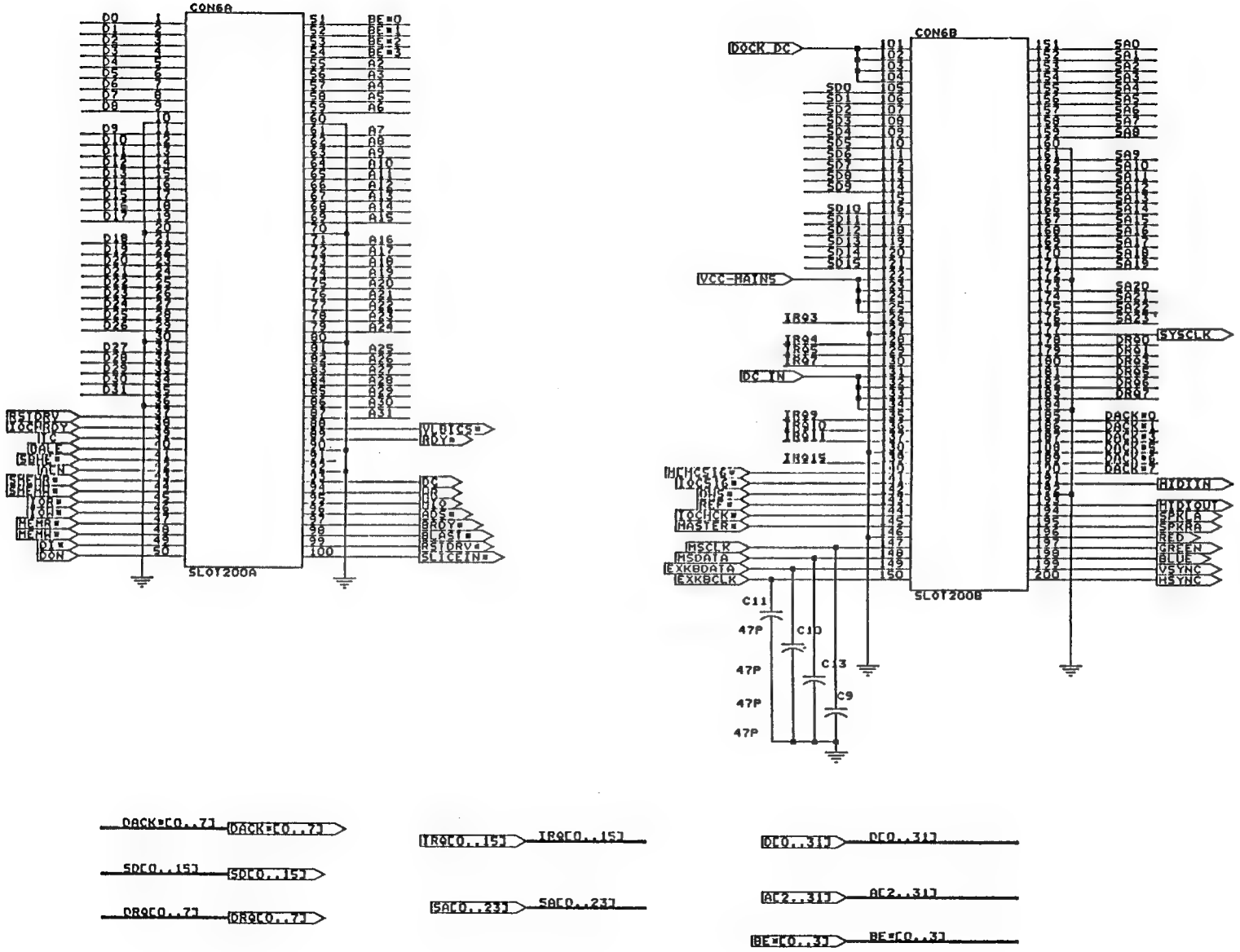


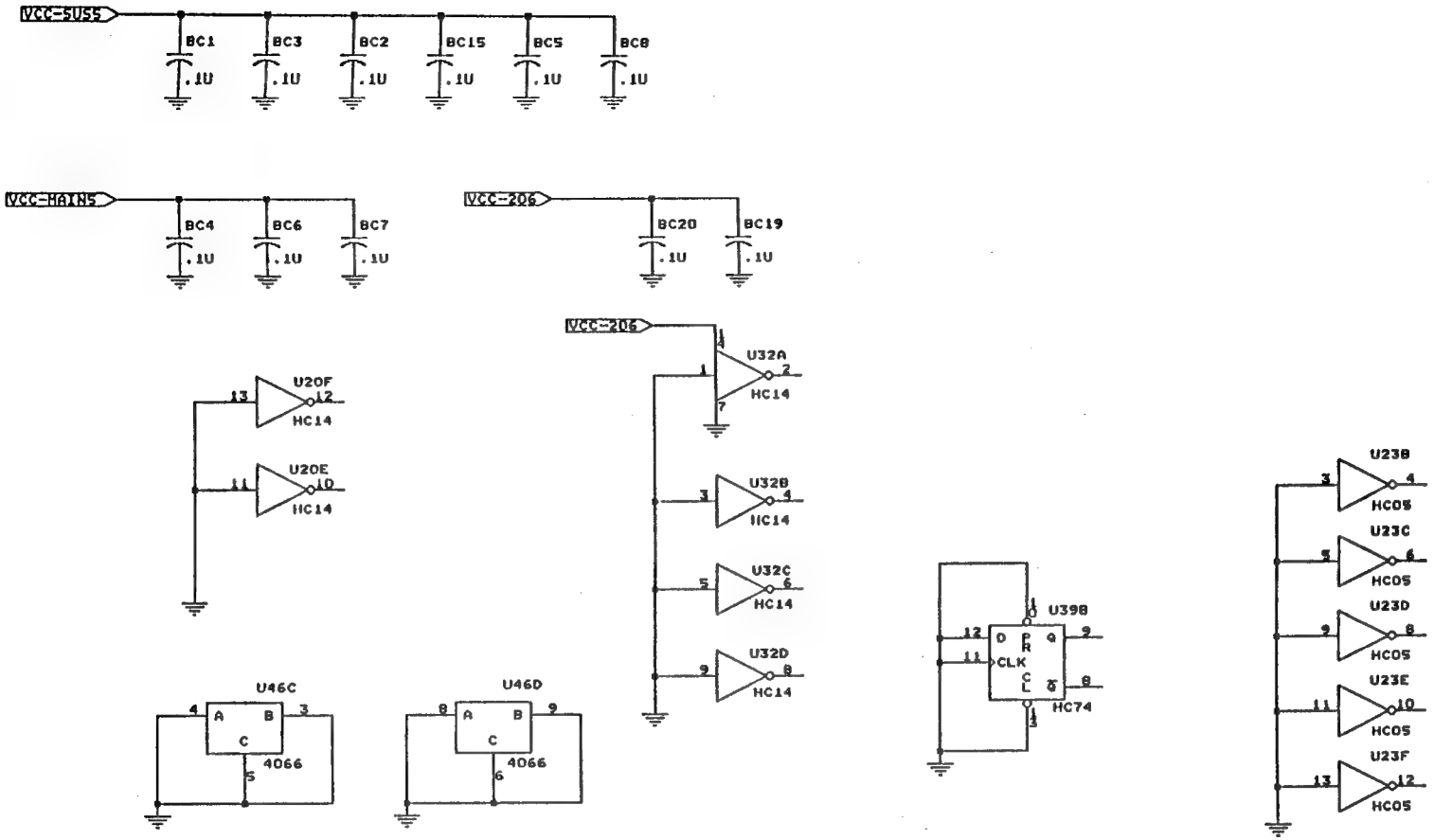


PK-486W/RTC power/Reset sequence circuit




U44
VCC-MAIN3
VCC-MAIN5
VCC-5US3
VCC-5US5
DY9956
C150
4.7U
C152
4.7U
+12V
R168
1M
QN5A
5USP
IMH9
VCC-EG3
VCC-MAIN3
ID_MAX= 3.5A 25° C
2.2A 100° C
U47
A_VCC_CARD
B_VCC_CARD
VCC-5US5
DY9956
+12V
R176
100K
QN1A
B_VCCEN#
IMH9
+12V
R179
100K
QN1B
A_VCCEN#
IMH9
VCC-MAIN5
D26
1N4148
+12V
Q14
2N3906
VCC-FLASH
R182
1K
R183
10K
C158
.1U
QN5B
FLASHROM
IMH9
+12V
R181
10K
R180
10K
QN2B
QN2A
BFPVCC
IMH9
U48
LCDVCC
VCC-FAN
VCC-5US5
VCC-MAIN5
DY9956
+12V
R153
1M
R147
1M
QN4B
QN4A
FANON
IMH9


CON6A
SLOT200A
CON6B
SLOT200B
DOCK_DC
VCC=MAIN5
IR03
IR04
IR05
IR07
DC_IN
IR09
IR010
IR011
IR015
MSCLK
MSDATA
EXKBDATA
EXKBCLK
C11
47P
C10
47P
C13
47P
C9
47P
SYSCLK
MIDIIN
MIDIOUT
SPKLA
SPKRA
RED
GREEN
BLUE
VSYNC
HSYNC
DACK=C0..7]
IRQC0..15]
SDC0..15]
SAC0..23]
DRQC0..7]
DC0..31]
AC2..31]
BE=C0..3]



VCC-5US5 U4(ACT245) U5(AC16245) U6(HC08) U9(HC14) U13(LM339) U17(HC08) U18(HC32) U19(HC32) U26(HC14) U27(HC08) U34(LM339) U46(4066) U50(HCT245)

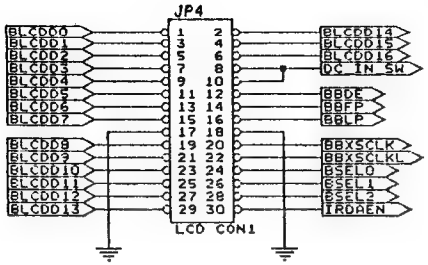
VCC-MAIN5 U20(HC14) U45(HCT245) U49(HCT245) U51(HCT245)

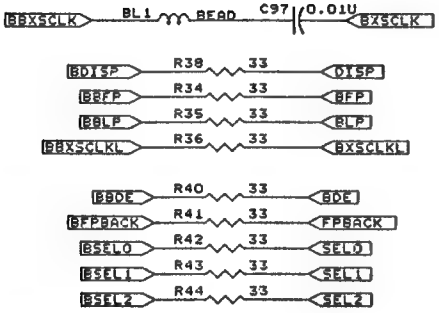
VCC-5US3

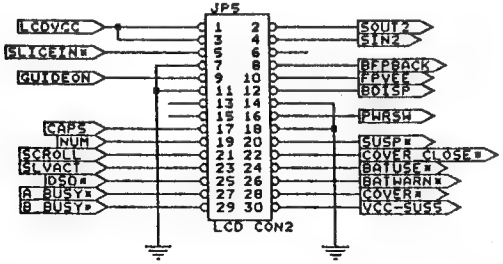
VCC-MAIN3 U2(LVT16245) U3(LVT16245) U7(LVT16245) U10(LVT16245) U35(LVT16245)

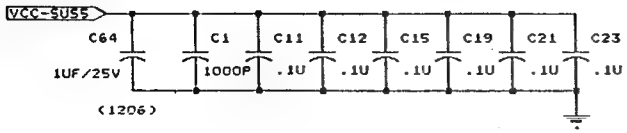
VCC-206 U14(4069) U32(HC14) U39(HC74)

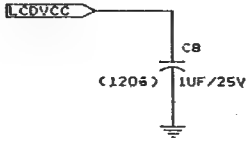
PK-LSP2/LCD/ICON CON

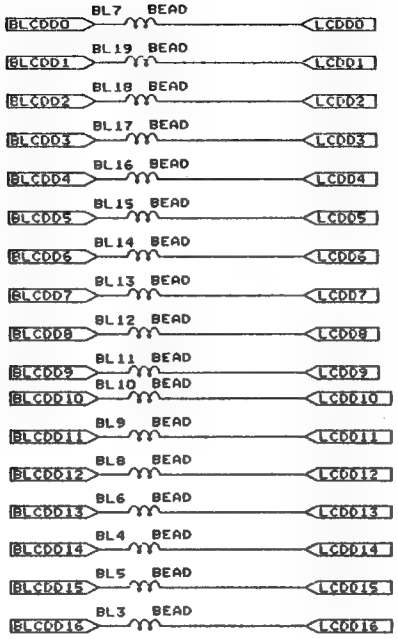


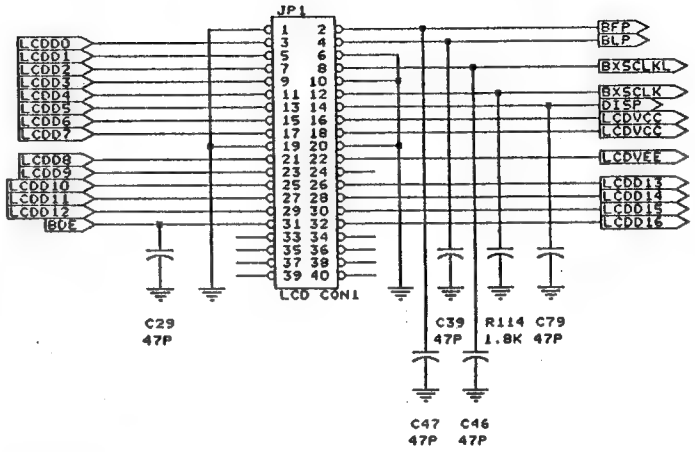


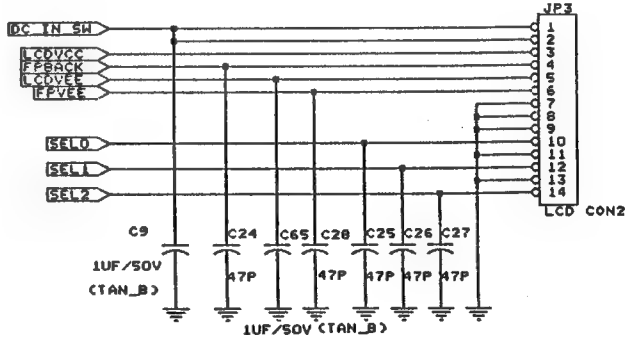




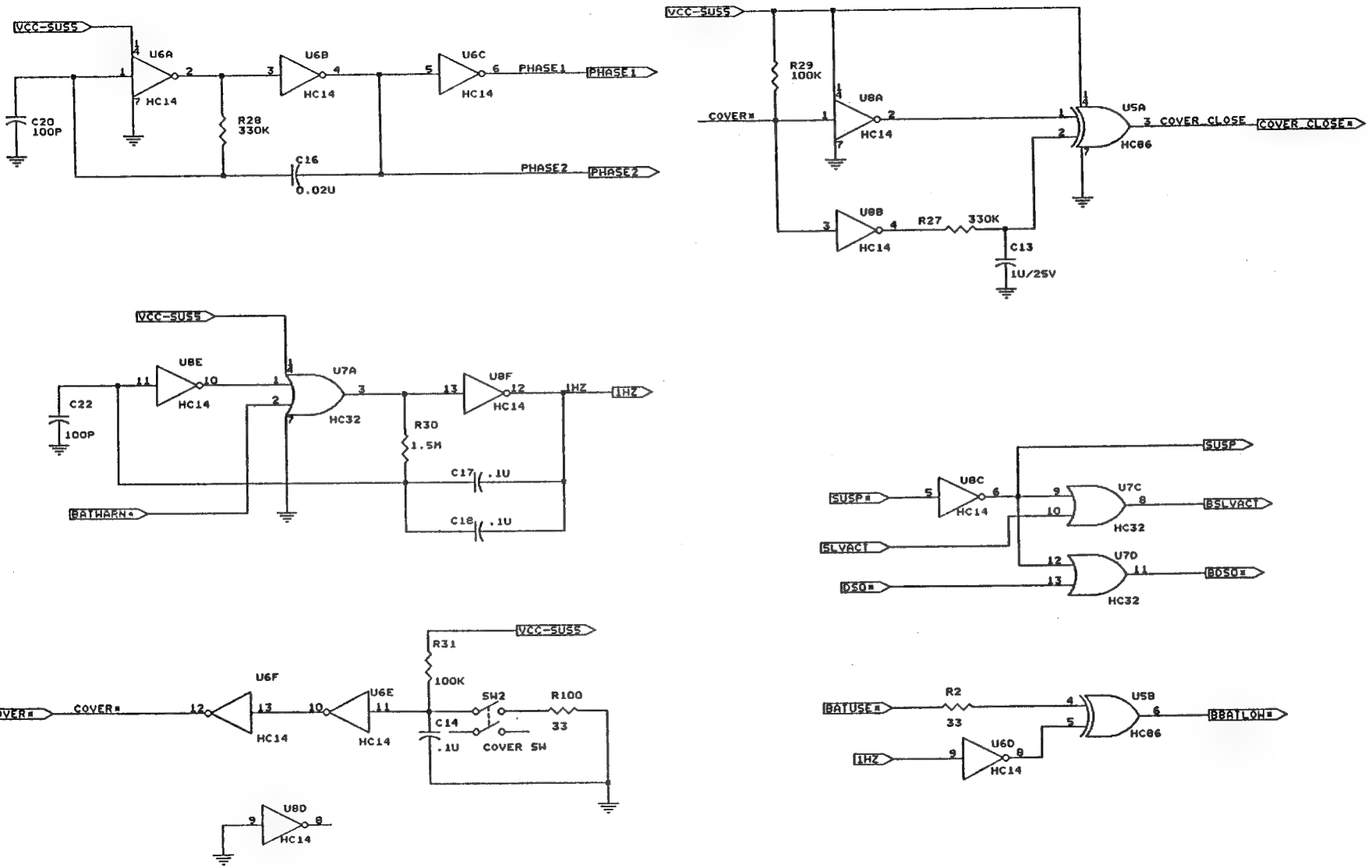


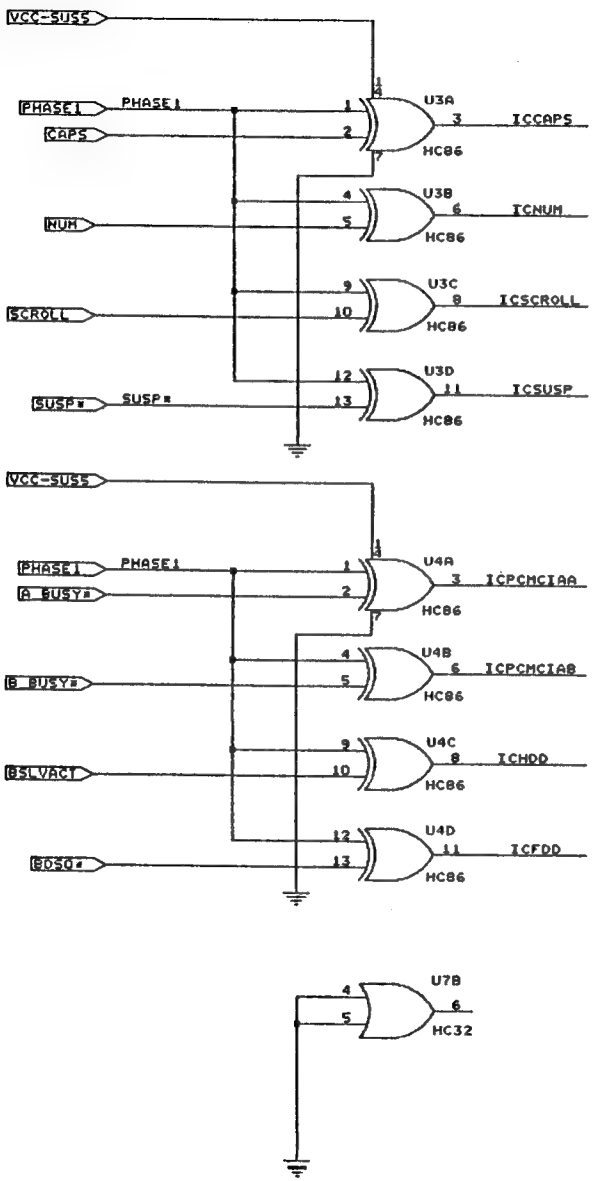


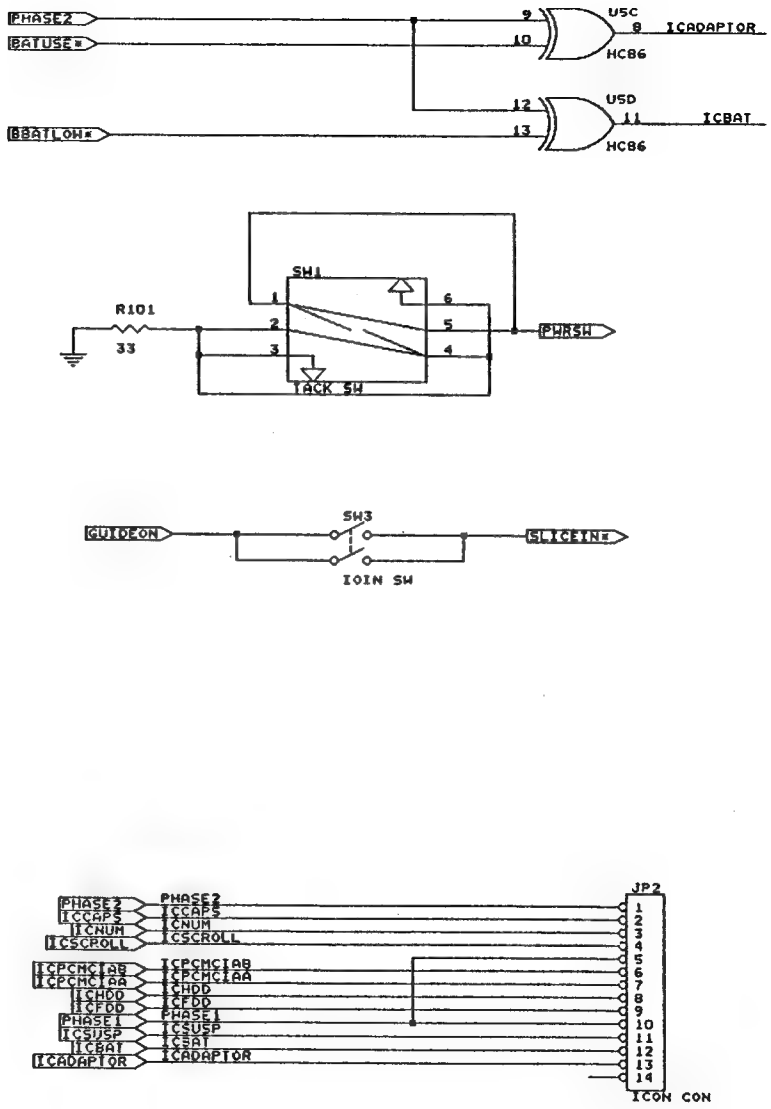


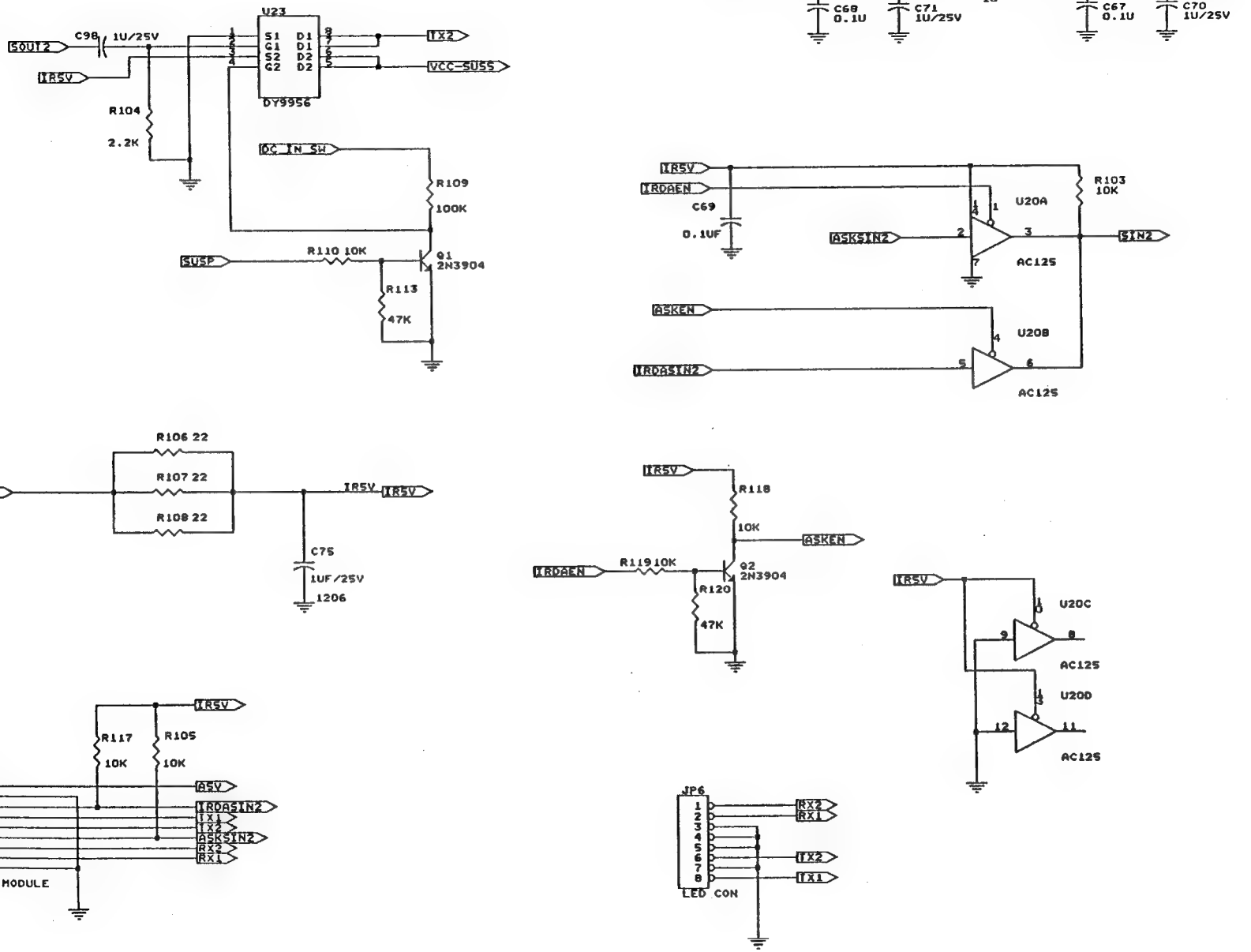


PIN 9-10	PIN 11-12	PIN 13,14	:	PANEL TYPE
OPEN	OPEN	OPEN	:	DSTN
CLOSE	OPEN	OPEN	:	MONO
OPEN	CLOSE	OPEN	:	TFT 9-BIT
CLOSE	CLOSE	OPEN	:	TFT 12-BIT
CLOSE	CLOSE	CLOSE	:	TFT 18-BIT

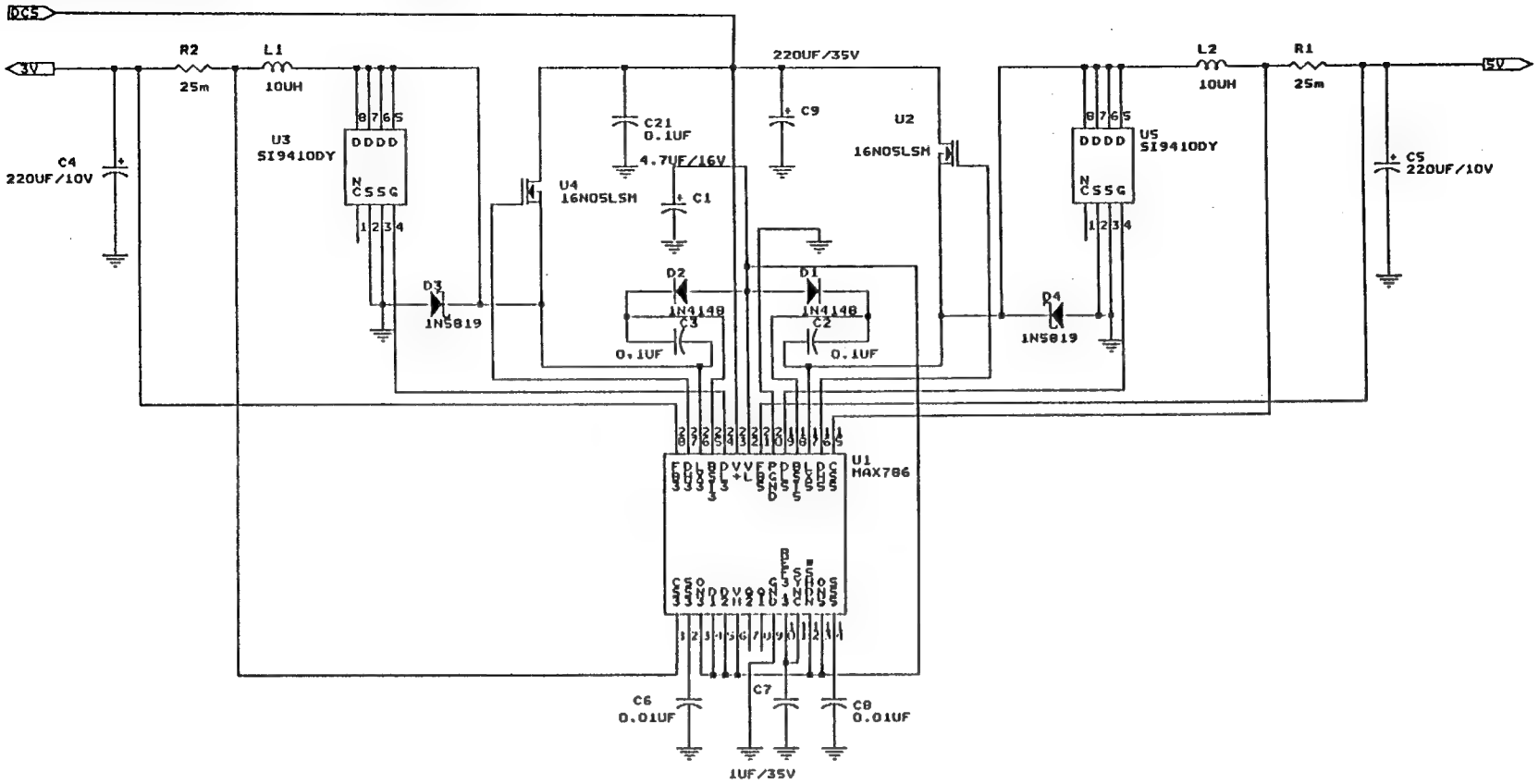

VCC-SUSS
U6A
HC14
U6B
HC14
U6C
HC14
PHASE1
PHASE1
C20
100P
R28
330K
C16
0.02U
PHASE2
PHASE2
VCC-SUSS
R29
100K
COVER*
U8A
HC14
U5A
HC86
3 COVER CLOSE
COVER CLOSE*
U8B
HC14
R27
330K
C13
1U/25V
VCC-SUSS
U8E
HC14
U7A
HC32
U8F
HC14
1HZ
1HZ
C22
100P
R30
1.5M
C17 .1U
C18 .1U
BATWARN*
SUSP
U8C
HC14
SUSP*
U7C
HC32
BSLVACT
SLVACT
U7D
HC32
BDSO*
DSO*
VCC-SUSS
R31
100K
U6F
HC14
U6E
HC14
SW2
R100
33
C14
.1U
COVER SW
COVER*
COVER*
U8D
HC14
BATUSE*
R2
33
U5B
HC86
BBATLOW*
1HZ
U6D
HC14

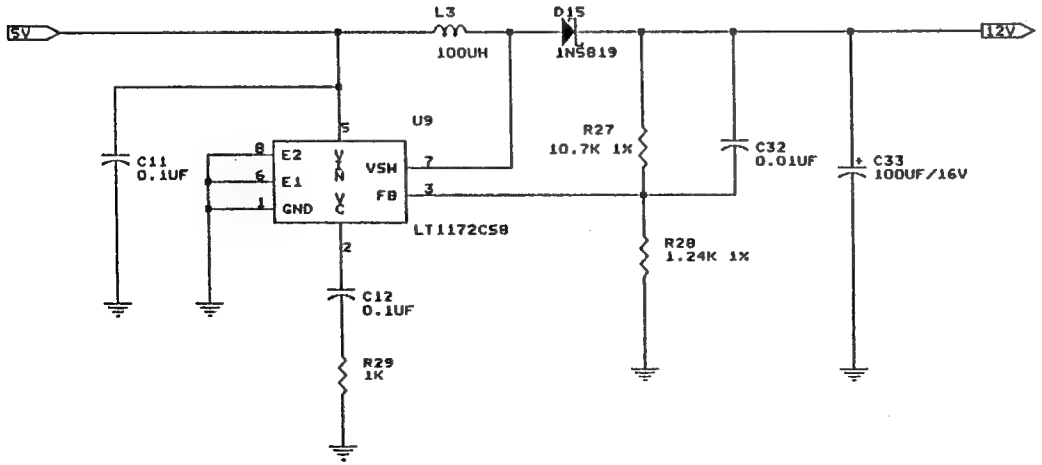

VCC-SUSS
PHASE1
PHASE1
CAPS
NUM
SCROLL
SUSP*
SUSP*
U3A
U3B
U3C
U3D
HC86
ICCAPS
ICNUM
ICSCROLL
ICSUSP
VCC-SUSS
PHASE1
PHASE1
A BUSY*
B BUSY*
BSLVACT
BDSQ*
U4A
U4B
U4C
U4D
HC86
ICPCMCIAA
ICPCMCIAB
ICHDD
ICFDD
U7B
HC32

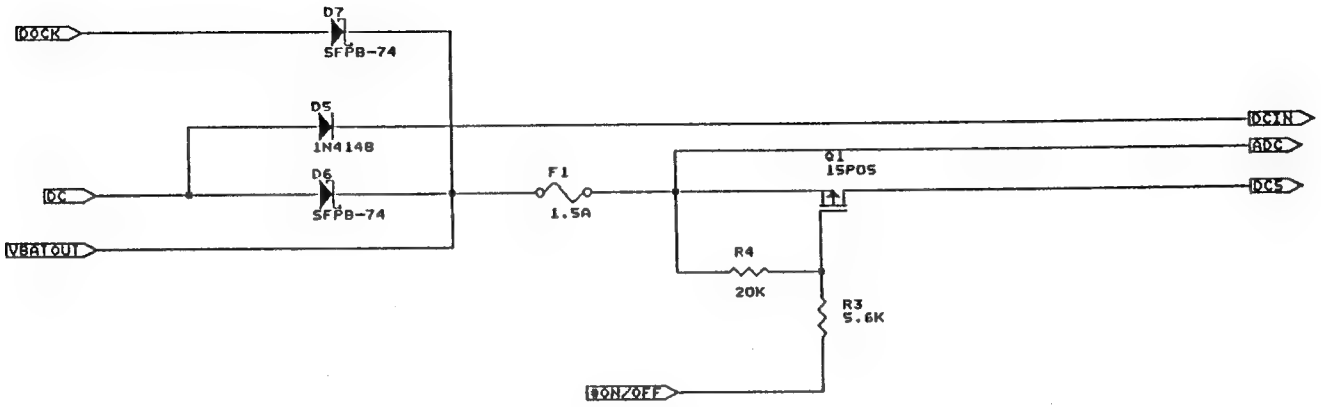

PHASE2
BATUSE*
BBATLOW*
U5C
U5D
HC86
ICADAPTOR
ICBAT
SW1
R101
33
TACK SW
PWRSW
SW3
GUIDEON
SLICEIN*
IOIN SW
JP2
PHASE2
ICCAPS
ICNUM
ICSCROLL
ICPCMCIAB
ICPCMCIAA
ICHDD
ICFDD
PHASE1
ICSUSP
ICBAT
ICADAPTOR
ICON CON

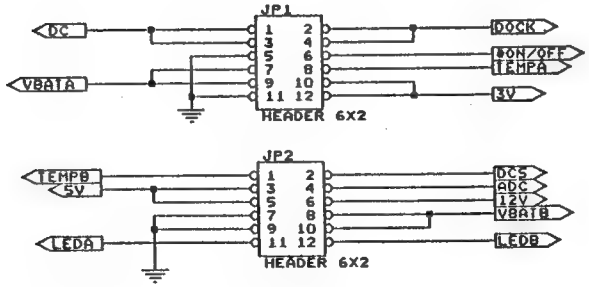

R102
10
IR5V
A5V
C68
0.1U
C71
1U/25V
C67
0.1U
C70
1U/25V
U23
S1
G1
S2
G2
D1
D1
D2
D2
DY9956
SOUT2
C98
1U/25V
IR5V
TX2
VCC-SUSS
R104
2.2K
DC_IN_SW
R109
100K
SUSP
R110 10K
Q1
2N3904
R113
47K
IR5V
IRDAEN
C69
0.1UF
U20A
R103
10K
ASKSIN2
SIN2
AC125
ASKEN
U20B
IRDASIN2
AC125
R106 22
R107 22
R108 22
TX1
IR5V
IR5V
C75
1UF/25V
1206
IR5V
R118
10K
ASKEN
IRDAEN
R119 10K
Q2
2N3904
R120
47K
IR5V
U20C
AC125
U20D
AC125
IR5V
R117
10K
R105
10K
JP7
A5V
IRDASIN2
TX1
TX2
ASKSIN2
RX2
RX1
DASK MODULE
JP6
RX2
RX1
TX2
TX1
LED CON

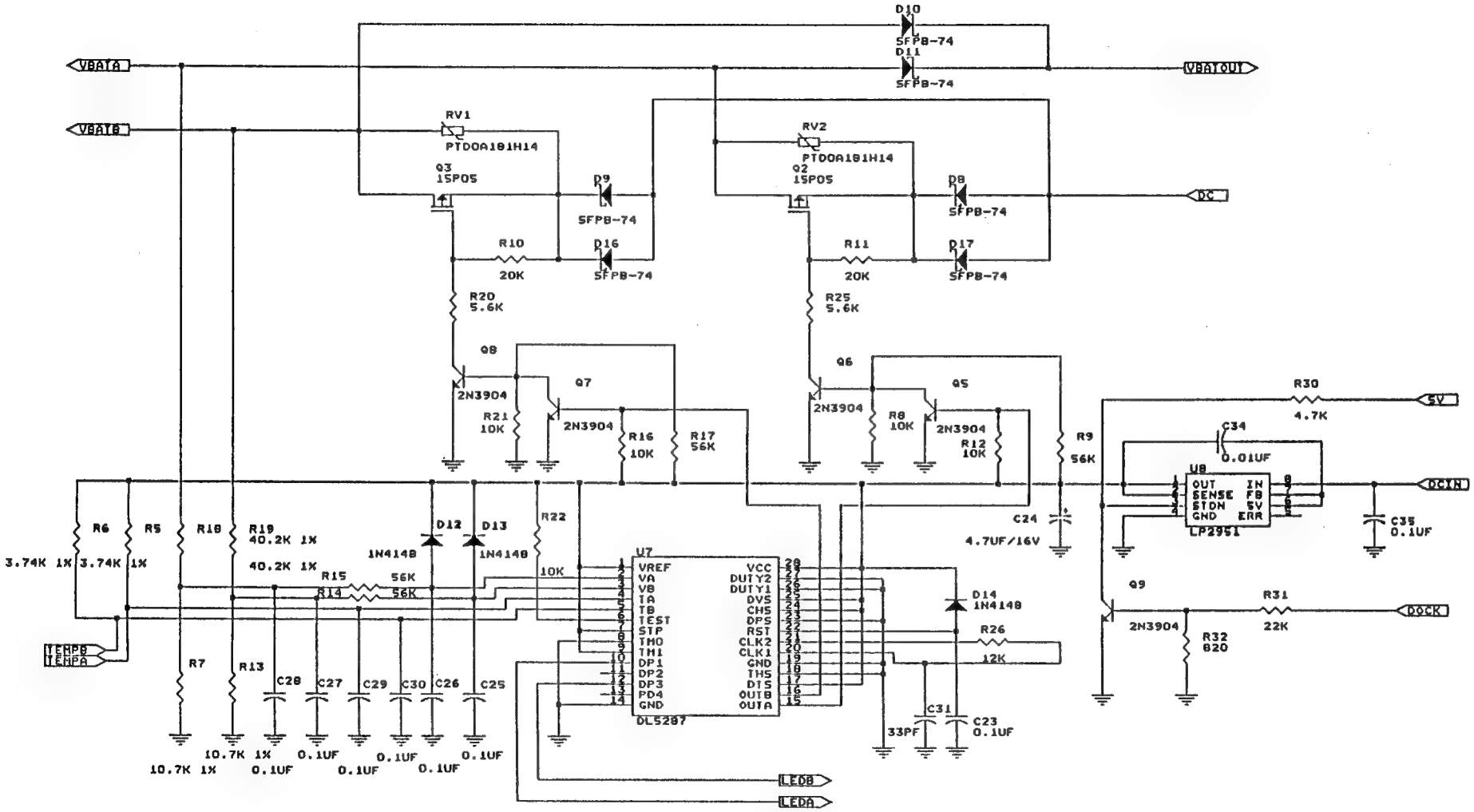
PK-DC/Power supply 3V & 5V for slim III

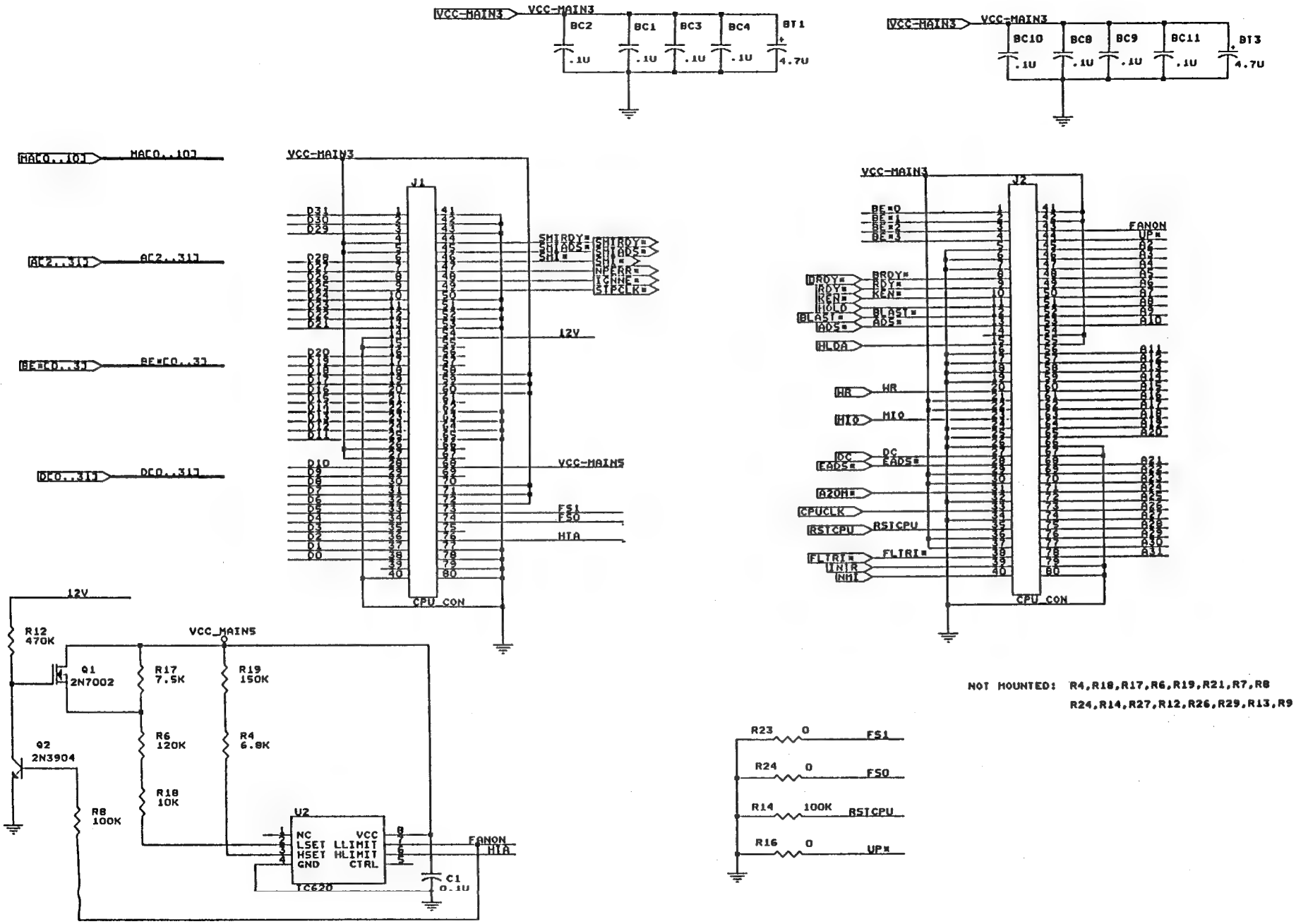




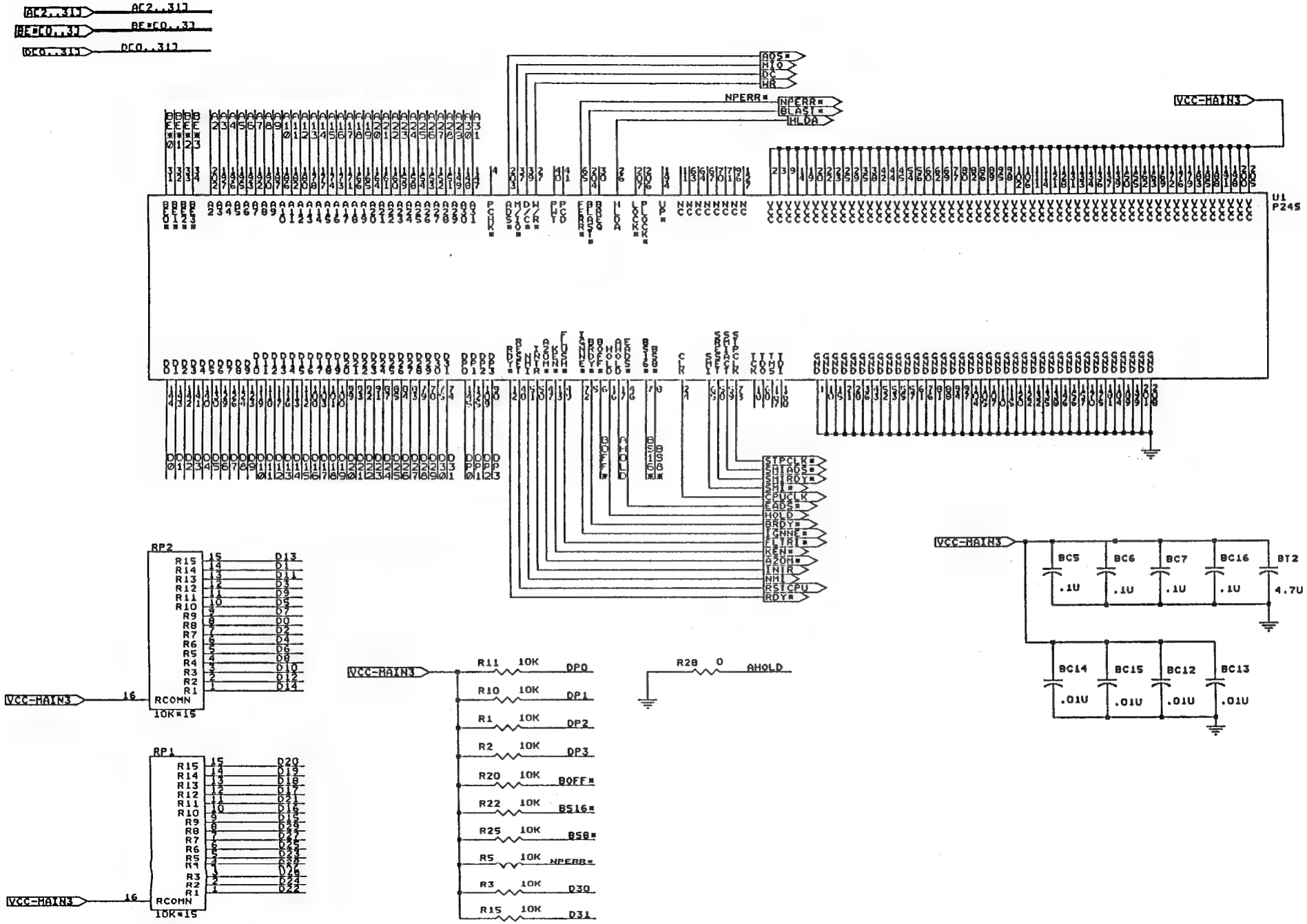

DOCK
D7
SFPB-74
D5
1N4148
D6
SFPB-74
DC
VBATOUT
F1
1.5A
Q1
1SP05
R4
20K
R3
5.6K
ON/OFF
DCIN
ADC
DCS

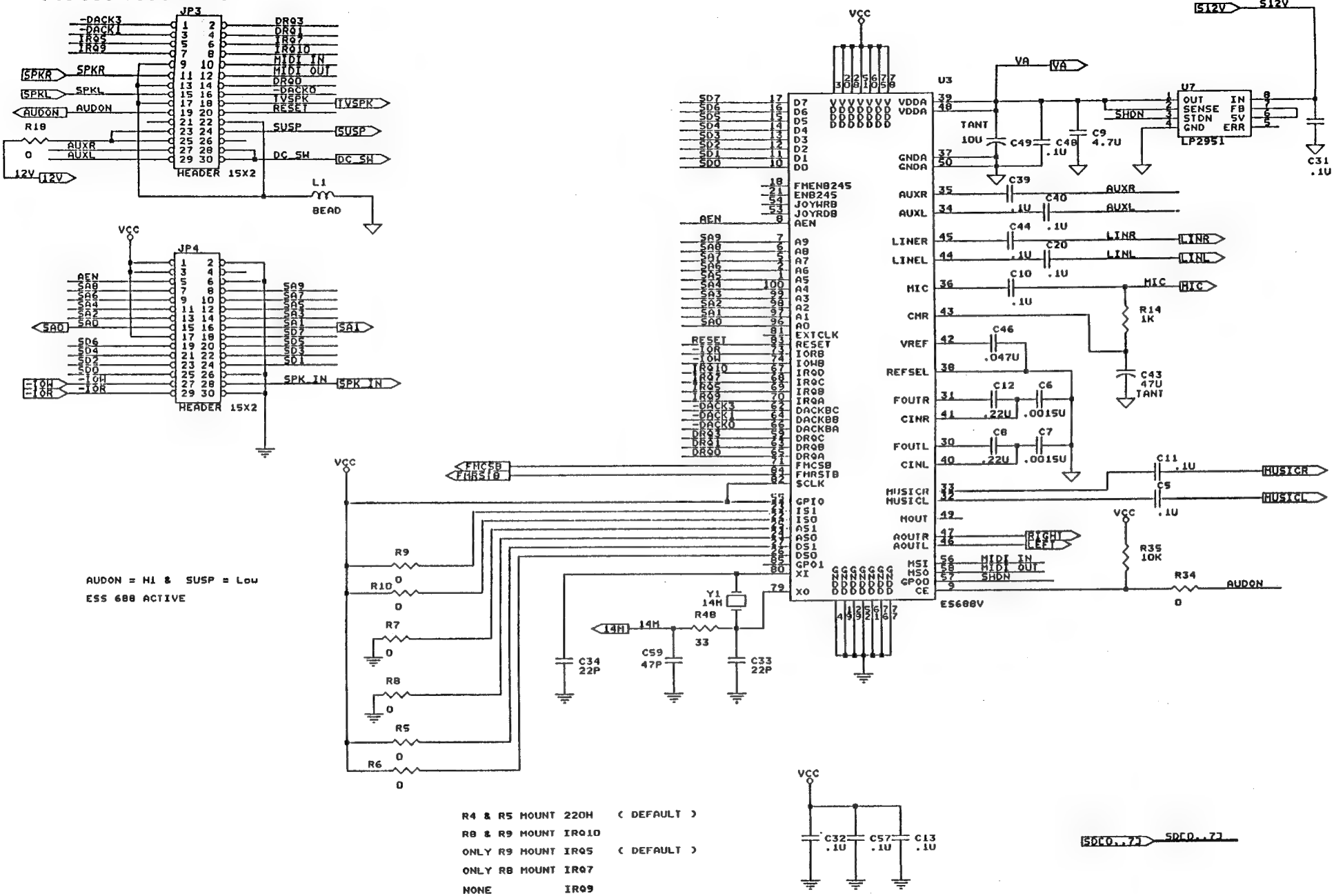

JP1
DC
VBATA
DOCK
ON/OFF
TEMPA
3V
HEADER 6X2
JP2
TEMPB
5V
LEDA
DCS
ADC
12V
VBATB
LEDB
HEADER 6X2

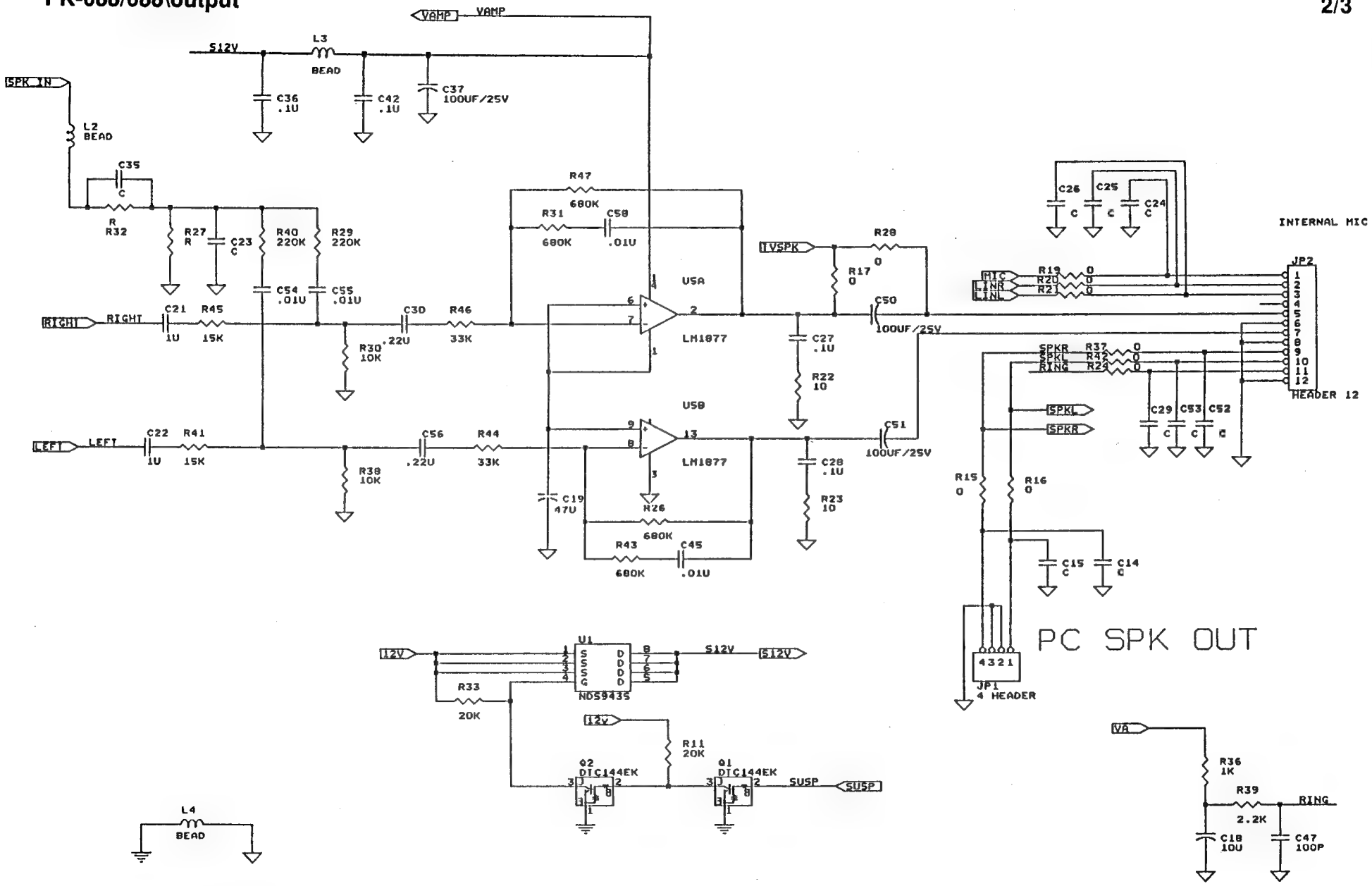

VBATA
VBATB
VBATOUT
D10
SFPB-74
D11
SFPB-74
RV1
PTD0A101H14
RV2
PTD0A101H14
Q3
1SP05
Q2
1SP05
D9
SFPB-74
D8
SFPB-74
DC
R10
20K
D16
SFPB-74
R11
20K
D17
SFPB-74
R20
5.6K
R25
5.6K
Q8
2N3904
Q7
2N3904
Q6
2N3904
Q5
2N3904
R21
10K
R16
10K
R17
56K
R8
10K
R12
10K
R9
56K
R30
4.7K
5V
C34
0.01UF
U8
OUT
SENSE
STDN
GND
IN
FB
5V
ERR
LP2951
DCIN
C35
0.1UF
C24
4.7UF/16V
R6
3.74K 1%
R5
3.74K 1%
R18
R19
40.2K 1%
40.2K 1%
D12
1N4148
D13
1N4148
R22
10K
R15
56K
R14
56K
U7
VREF
VA
VB
TA
TB
TEST
STP
TMD
TM1
DP1
DP2
DP3
PD4
GND
VCC
DUTY2
DUTY1
DVS
CHS
DPS
RST
CLK2
CLK1
GND
THS
DTS
OUTB
OUTA
DL5287
D14
1N4148
R26
12K
Q9
2N3904
R31
22K
DOCK
R32
820
TEMPB
TEMPA
R7
10.7K 1%
R13
10.7K 1%
C28
0.1UF
C27
0.1UF
C29
0.1UF
C30
0.1UF
C26
0.1UF
C25
0.1UF
C31
33PF
C23
0.1UF
LEDB
LEDA



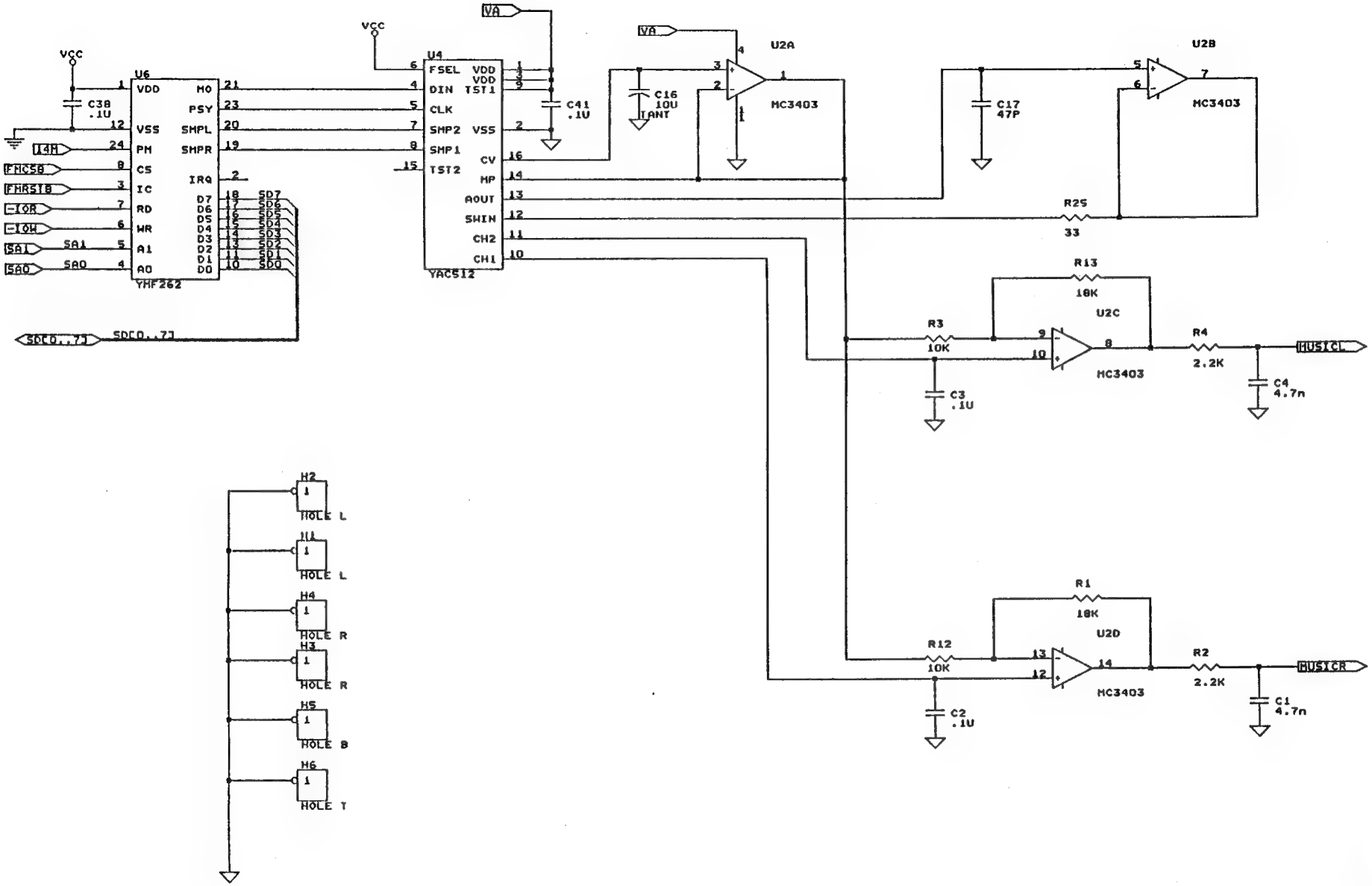
NOT MOUNTED: R4,R18,R17,R6,R19,R21,R7,R8
R24,R14,R27,R12,R26,R29,R13,R9

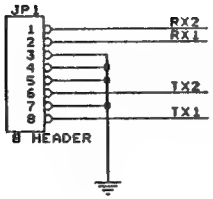

AD2..31
BE#0..3
DP0..3
ADS#
M/IO
D/C
W/R
NPERR
NPERR#
BLAST#
HLDA
VCC-MAIN3
U1
P245
STPCLK#
SMIADS#
SMIRQY#
SMI#
CPUCLK
EADS#
HOLD
BRDY#
IGNNE#
FLUSH#
KEN#
A20M#
INTR
NMI
RSTCPU
RDY#
RP2
RCOMN
10K*15
D13
D1
D11
D3
D9
D5
D7
D0
D2
D4
D6
D8
D10
D12
D14
RP1
D20
D19
D18
D17
D21
D16
D15
D23
D25
D24
D22
R11 10K DP0
R10 10K DP1
R1 10K DP2
R2 10K DP3
R20 10K B0FF#
R22 10K BS16#
R25 10K BS8#
R5 10K NPERR#
R3 10K D30
R15 10K D31
R28 0 AHOLD
BC5 .1U
BC6 .1U
BC7 .1U
BC16 .1U
BT2 4.7U
BC14 .01U
BC15 .01U
BC12 .01U
BC13 .01U

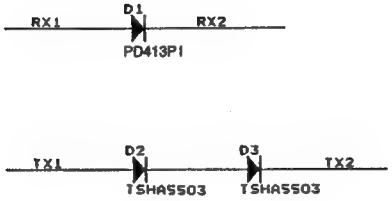

JP3
HEADER 15X2
JP4
HEADER 15X2
U3
ES688V
U7
LP2951
AUDON = Hi & SUSP = Low
ESS 688 ACTIVE
R4 & R5 MOUNT 220H (DEFAULT)
R8 & R9 MOUNT IRQ10
ONLY R9 MOUNT IRQ5 (DEFAULT)
ONLY R8 MOUNT IRQ7
NONE IRQ9
R6 & R7 MOUNT DMA3
ONLY R6 MOUNT DMA1 (DEFAULT)
ONLY R7 MOUNT DMA0



*** NOTE ***
THE ANALOG GROUND AND DIGITAL GROUND
IS CONNECTED THROUGH THIS FERRITE BEAD

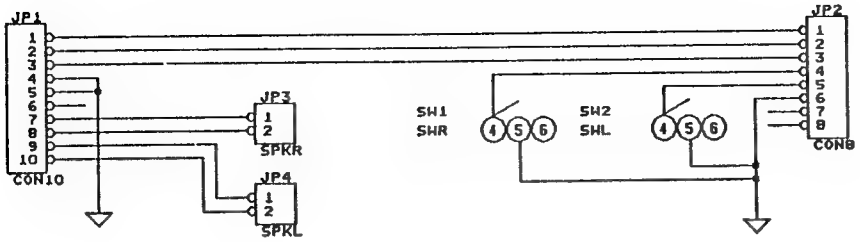

VCC
U6
VDD
C38
.1U
VSS
I4M
PM
FNCSB
CS
FHRSTB
IC
-IOR
RD
-IOW
WR
SA1
A1
SA0
A0
MO
PSY
SMPL
SMPR
IRQ
D7
D6
D5
D4
D3
D2
D1
D0
YMF262
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
SDC0..7]
VA
U4
FSEL
DIN
CLK
SMP2
SMP1
TST2
VDD
TST1
VSS
CV
MP
AOUT
SHIN
CH2
CH1
YAC512
C41
.1U
C16
10U
TANT
U2A
MC3403
C17
47P
U2B
R25
33
R13
10K
U2C
R3
10K
R4
2.2K
MUSICL
C3
.1U
C4
4.7n
R1
10K
U2D
R12
10K
R2
2.2K
MUSICR
C2
.1U
C1
4.7n
H2
HOLE L
H1
HOLE L
H4
HOLE R
H3
HOLE R
H5
HOLE B
H6
HOLE T


JP1
1
2
3
4
5
6
7
8
8 HEADER
RX2
RX1
TX2
TX1


D1
RX1
RX2
PD413P1
D2
D3
TX1
TX2
TSHA5503
TSHA5503

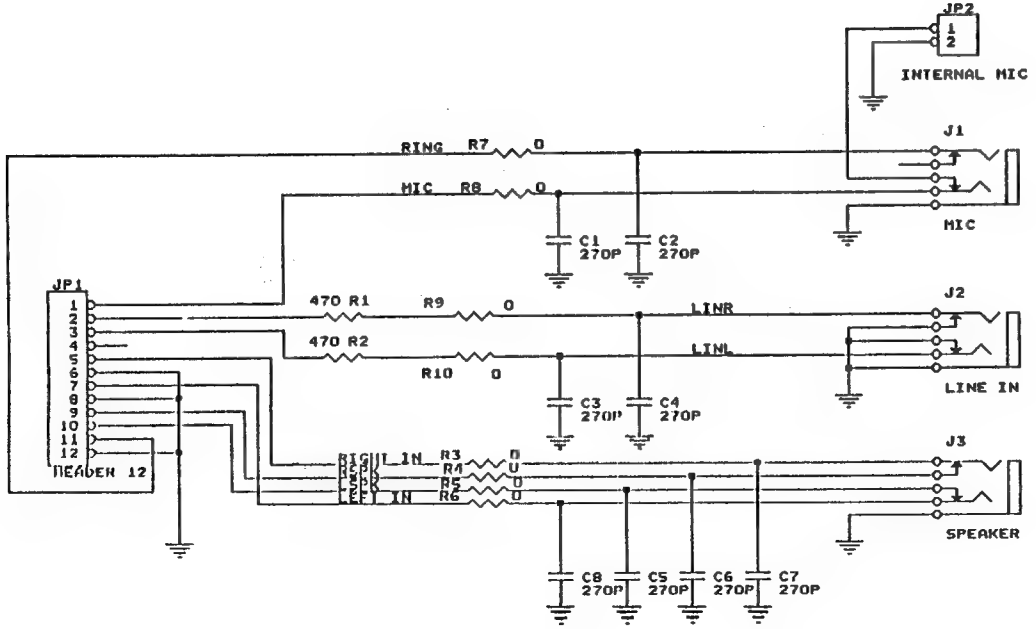
PK-GPT

1/1



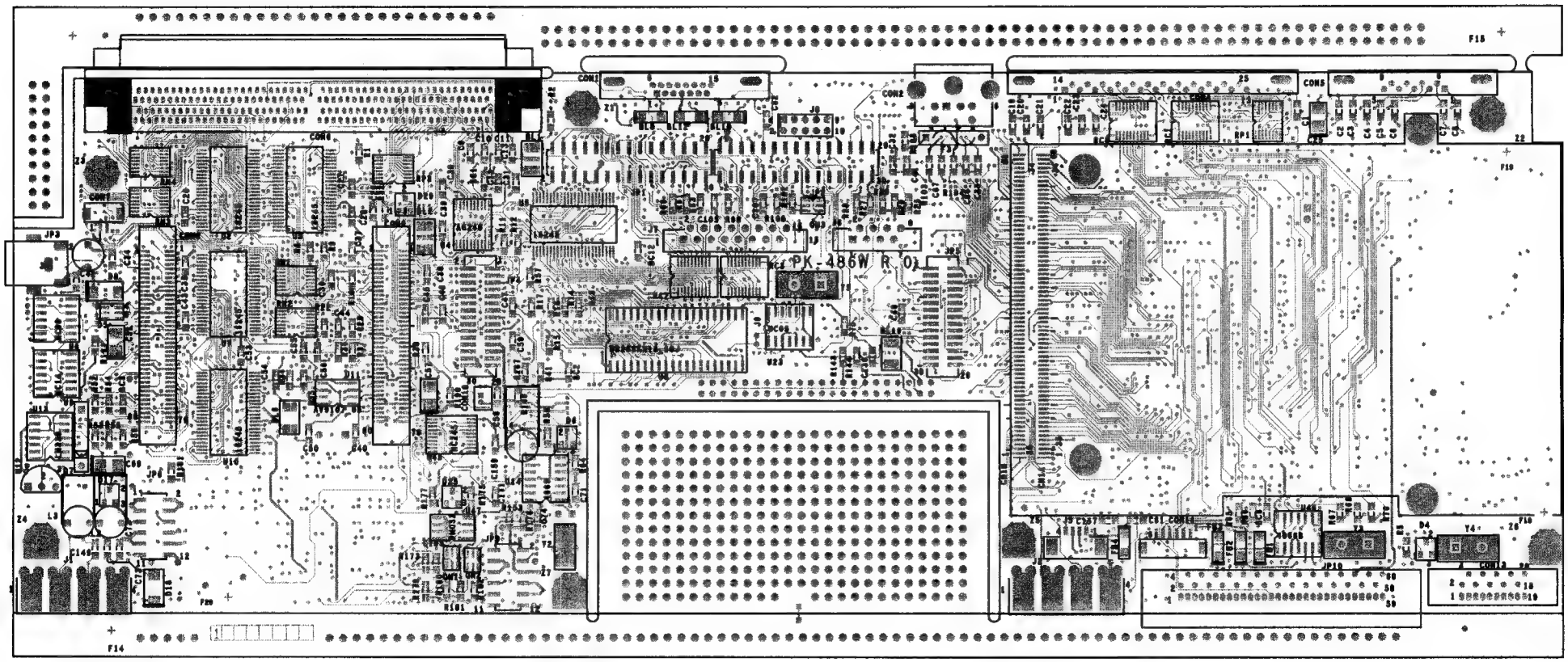
PK-AUD

1/1

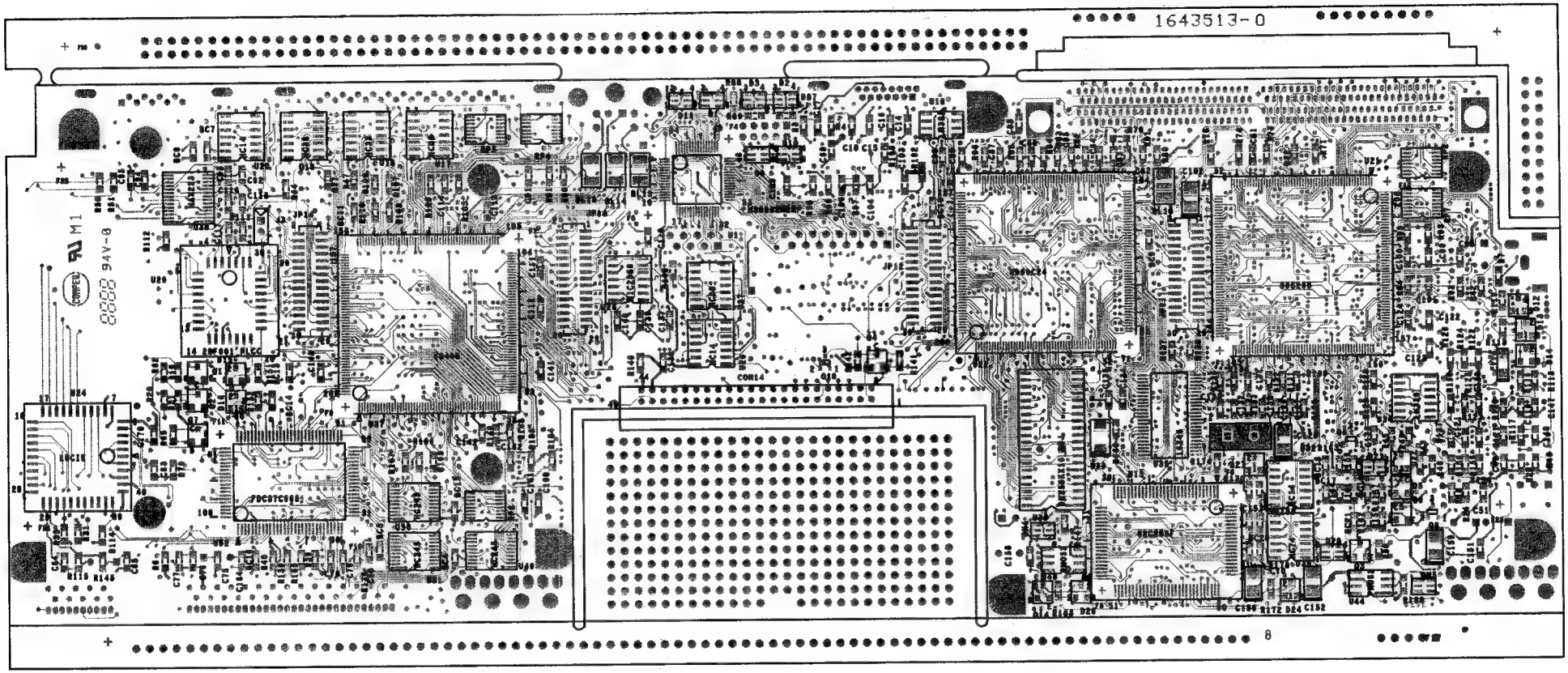


PARTS LAYOUT

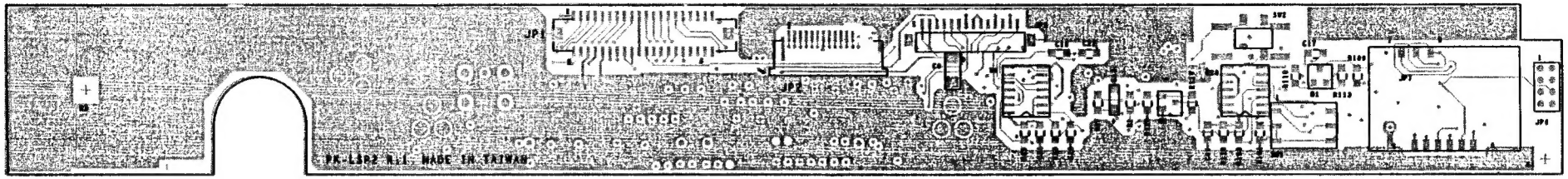
PK-486W(1/2)



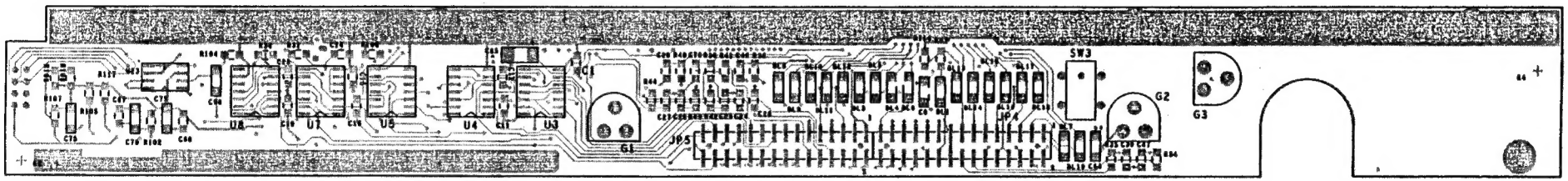
PK-486W(2/2)



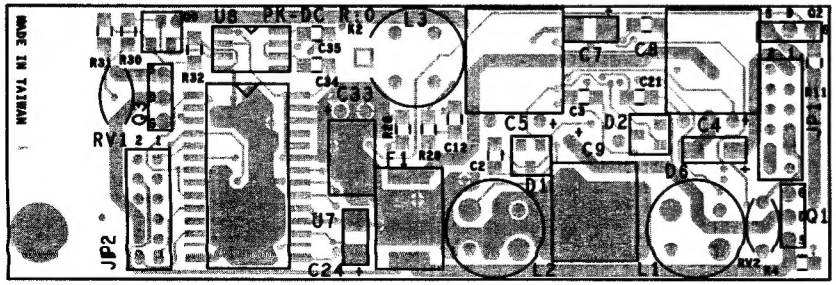
PK-LSP2 (1/2)



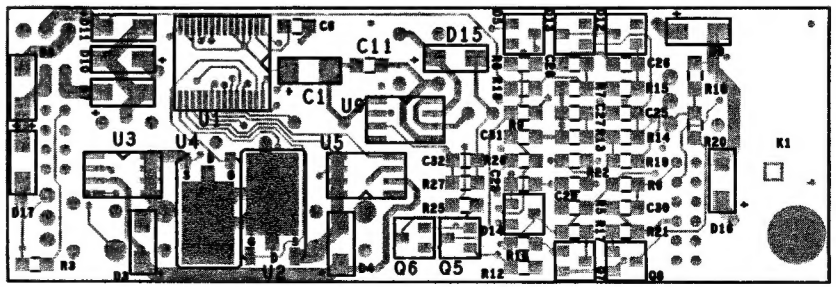
PK-LSP2 (2/2)



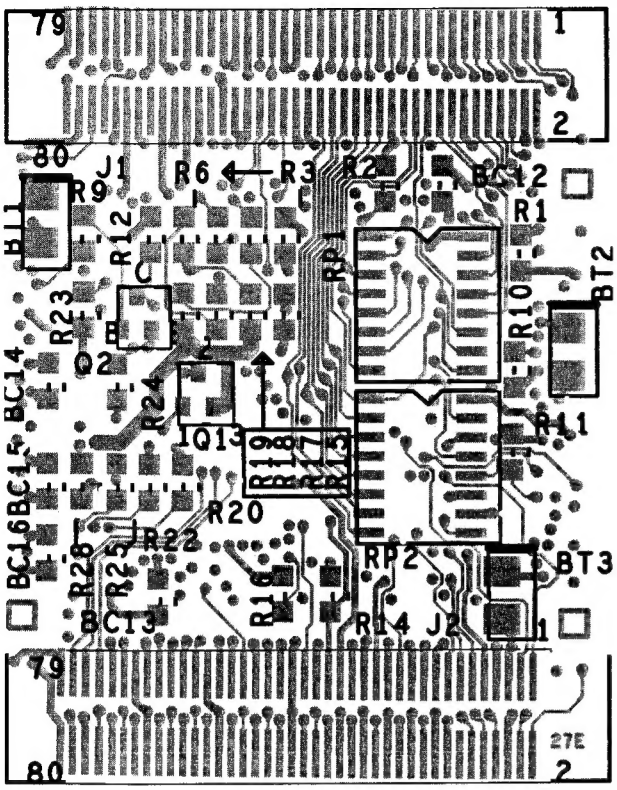
PK-DC (1/2)



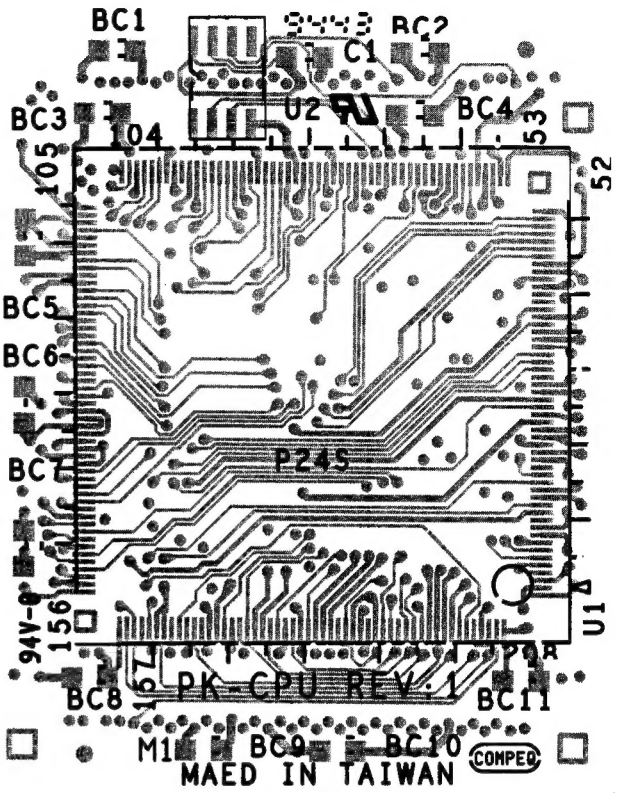
PK-DC (2/2)



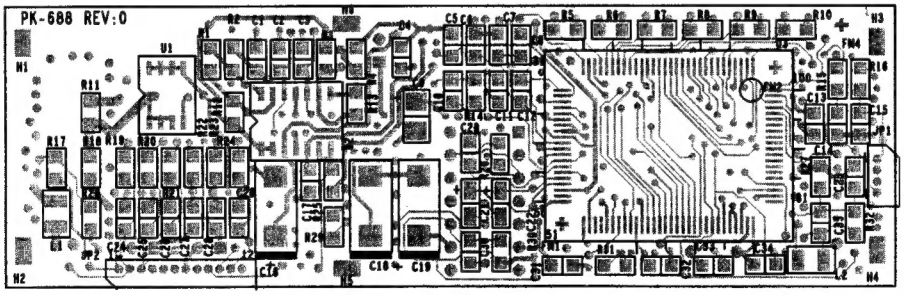
PK-CPU (1/2)



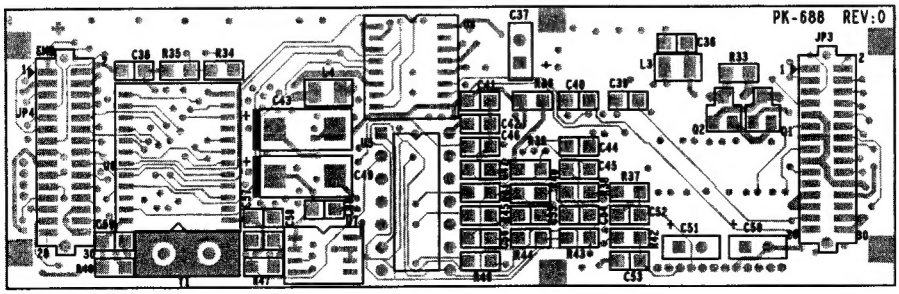
PK-CPU (2/2)



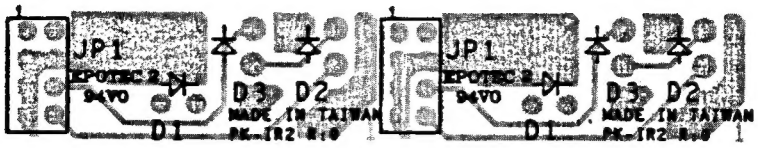
PK-688 (1/2)



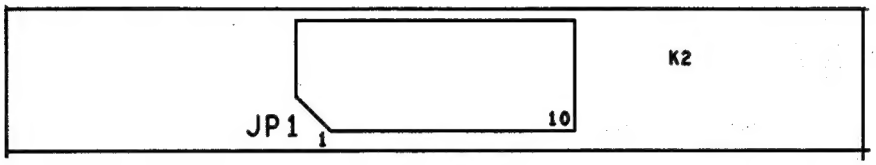
PK-688 (2/2)



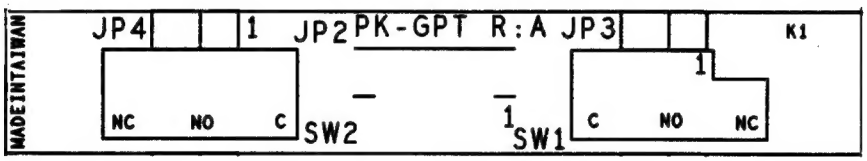
PK-IR2



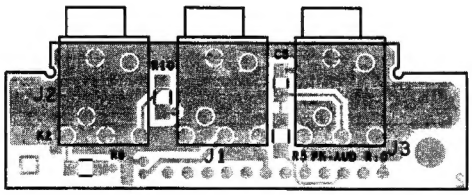
PK-GPT (1/2)



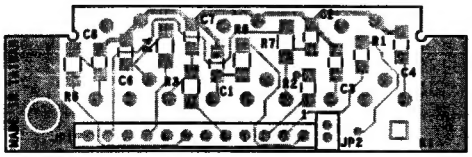
PK-GPT (2/2)



PK-AUD (1/2)



PK-AUD (2/2)



SHARP

PERSONAL COMPUTER: PC-8700/8900

Date: Dec. 18, 1995

No. : TTE-157

Technical Report

[Parts changes]

CHANGE OF THE FDD

1. Model name: PC-8700/8900

2. Description: The production of the FDD made by Cannon was disused and the substitute by NEC has been used.

Accordingly the relative parts have also been changed as follows.

3. Parts change:

Ref No.	Model name	Version	P/G No.	Current parts	New parts		Parts name	Effective time	Interchangeability	Note
				Parts code	Parts code	Price rank				
1	PC-8700 PC-8900	All	[2]-35	0JS7001314427	0JS7001314433	BZ	2 mode FDD	Mar. '95	5	—
2			[2]-36	0JS5002032302	0JS5002041702	AM	FDD BOX			
3			—	—	0JS4181012004	AC	Screw			

<Interchange>

1. Interchangeable.	4. Not interchangeable.
2. Current type can be used in place of new type. New type cannot be used in place of current type.	5. Interchangeable if replaced with same types of related parts in use.
3. Current type cannot be used in place of new type. New type can be used in place of current type.	6. Others.

Parts marked with "⚠" is important for maintaining the safety of the set.
Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.